Predicting, Validating, and Improving Yield of Multi-Chip RF Modules During Product Development

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***Abstract*—Providing product yield estimates during the NPD (New Product Development) life cycle is frequently required. Predicting these yields is very difficult and often based on a limited data set or no specific data whatsoever. These estimates are used for a wide range of critical business purposes including cost modeling, capacity planning, component supply, customer bids, personnel staffing, and factory utilization. Yield estimates for RFIC Multi-Chip modules are particularly difficult as these modules contain many sub components and a variety of technologies. A wide body of knowledge already exists regarding yield prediction and management for non-RF ICs. In this paper methods are discussed for modeling and validating RF module yield throughout product development. From the early concept phase to volume production, various techniques are proposed in an effort to provide accurate yield estimation and ensure RFIC modules launch with predictable and acceptable yields.**

I. Introduction

PROVIDING yield estimates early in Product Definition is often required for business purposes. Predicting these yields is very difficult and often based on a limited data set. These estimates are used for a wide range of purposes including: estimating profit margins, factory utilization, capacity planning, component supply studies, material logistics, customer bids, personnel staffing. Yield estimates for RFIC Multi-Chip modules is particularly complex as the modules contain many sub components and a variety of technologies. A typical RFIC module is shown in Fig 1.

The module shown in Fig 1 has many sub components including a Gallium Arsenide semiconductor die as shown by the power amplifier symbol (two triangles), a SAW (surface acoustic wave) filter shown on the RF input of the module, a pHEMT bias and power detector die, and a SAW duplexer. The subcomponents shown are attached to a multi-layer laminate along with a multitude of surface mount capacitors, inductors, and resistors. Fig 2 shows a RFIC multi-chip module as assembled before over molding.

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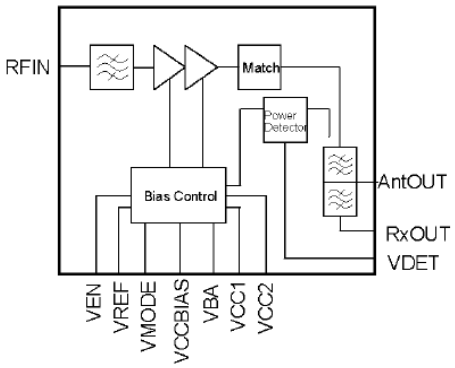


Fig 1: Typical RFIC module showing sub components

During the Design Phase, yield estimates begin to be improved through modeling and simulation, analyzing first articles, and early engineers design revisions ("design spins"). It is in the Product Verification Phase that yield estimates are initially verified. During this phase data from RFIC modeling and simulations are combined with empirical data from multiple hardware builds.

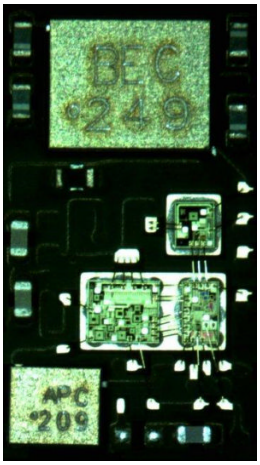


Fig 2: RFIC multi-chip module as assembled

During the Pilot Production Phase predictions about process variation, manufacturing variation, and design interaction become validated. The Pilot Production Phase involves the manufacturing of product ramp quantities consisting of many

wafer lots, SMD batches, and laminate batches. These builds tend to capture the majority of the "day to day" variation throughout the process.

Launching products with high yield is less about the topics presented in this paper and more about establishing a culture where high yields are expected by all team members and senior management. Achieving this deep focus is about a paradigm shift, from a "toss it over the fence" approach to a "we're all in this together" methodology.

II. PLANNING FOR HIGH YIELD DURING PRODUCT DEFINITION

Experiencing high yields during the production phase really starts early in the Product Definition phase. Fig 3 shows a typical New Product Development (NPD) flow. During this phase, it is critical that the definition team include development engineers focused on the long-term yield of the product. The role of Marketing during this phase is to build the business case for the product. Design Engineering's function is to make sure the concept is technically feasible. The role of Development Engineering is make sure the product yield assumptions are accurate considering the proposed target specifications, long-term variation of the manufacturing process, defect rates, process limitations, module complexity, guard banding, etc.

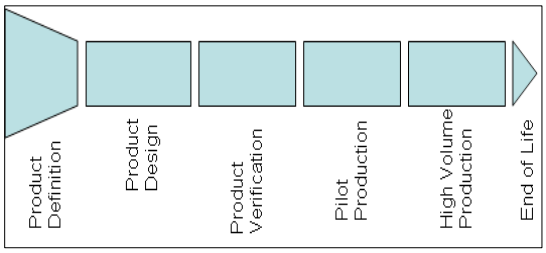


Fig 3: Typical new product development flow

In most cases, after the business case is approved, marketers begin engaging customers and establishing agreements regarding schedule, performance, and cost. If the cross functional definition team can identify potential yield challenges and process limitations early, the marketing team can spend more focus with customers early to address these issues, possibly adding margin to critical specs. By having a deep customer focus and understanding the limitations of the product early in NPD, a "win-win" scenario can often be realized, where customers get the product at an attractive price, profit margins hit target, and the supply risk due to yield variations is minimized.

From a high level, the flow described above sounds easy, but the "how-to" formula is more complex. Predicting yield during the product definition phase of multi-chip RFIC modules involves several strategies. First engineers review the target specifications and proposed architecture in detail and try to determine what Liebig's Law [1] calls "the limiting factor(s)" (also known as Yield Inhibitors). In RFIC PA modules, the limiting factor is typically specifications around linearity, gain, and current. In some cases the limiting factor may be process or materials related (e.g. fab process, assembly variation, test limitations). It is imperative during product definition that known limiting factors are discussed and strategies are developed to reduce the impact these factors.

A real-world example might be a linearity spec such as adjacent channel power (ACP). Based on process limitations and product architecture, engineers can predict the general performance of ACP. By identifying this limiting factor early in product development, marketing can work to define the specification in a way that is still competitive but provides as much margin as possible. Design can work to provide more design margin, process engineers can work on ways to improve the process, test engineers can work on ways to reduce test guard banding, and development engineers can work to comprehend all these aspects in an effort to plan for high yield before even one physical device exists.

The "how-to" formula for predicting product yield is farily simple. Getting organizations to "want-to" is sometimes more challenging. In a low volume / high margin businesses it is more difficult to get people to understand the importance of early yield planning & prediction. In high volume / low margin businesses every penny counts and yield is often the biggest lever impacting product profit margin.

Predicting yield inhibitors (limiting factors) during product definition is somewhat subjective. Engineers base predictions on performance of existing products, previous version performance (in the case of derivatives), and design targets. In order to predict yields, $\hat{C}_{pk}$ is calculated for each proposed parameter. $\hat{C}_{pk}$ is expressed as:

$$\hat{C}_{pk} = \min\left[\frac{USL - \hat{\mu}}{3\hat{\sigma}}, \frac{\hat{\mu} - LSL}{3\hat{\sigma}}\right]$$

Volume production data from several similar products can be helpful in establishing variation in the initial yield prediction. Distribution means ($\hat{\mu}$) are assumed to be based on early design targets. Distribution variation (expressed as standard deviation, $\hat{\sigma}$), assumes actual "production-like" variation, unless new technologies (i.e. design, process, test) are expected to provide reduced variation. Fig 4 depicts the customer requirements, defined during product definition, along with predicted guard bands and predicted distribution.

Predicted $\hat{C}_{pk}$ is calculated based on the predicted guard banded limits, expected design target $\hat{\mu}$ and "production-like" variation. Any parameter(s) which have a predicted $\hat{C}_{pk} < 2$ (99.99966%) require special attention during the design process. RFIC multi-chip modules typically have a large number of tests in production - (it's not uncommon to have 100+ production tests). Given just 50 tests, if we assume exclusive yield fallout, with each parameter yielding 99%, the overall yield would be 60.51%. This expression is shown below, where P_i is the yield of a given parameter:

$$\prod_{i=1}^{50} P_i$$

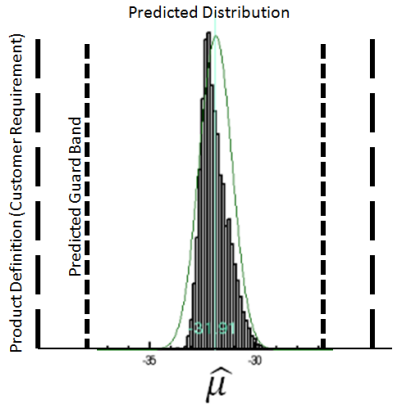


Fig 4: Illustration of Cpk Prediction

As can be seen in Fig 5, 99% is not a high enough expectation if high long term yields are desired. The figure shows an overall yield trend, considering 99% exclusive parametric yield for 150 tests. With a $\hat{C}_{pk} \geq 2$, the same 50 test exclusive yield would be 99.983%. $\hat{C}_{pk} \geq 2$ should be the goal early on in the development. Fig 5 shows overall yield, considering 99% exclusive parametric yield for 150 tests.

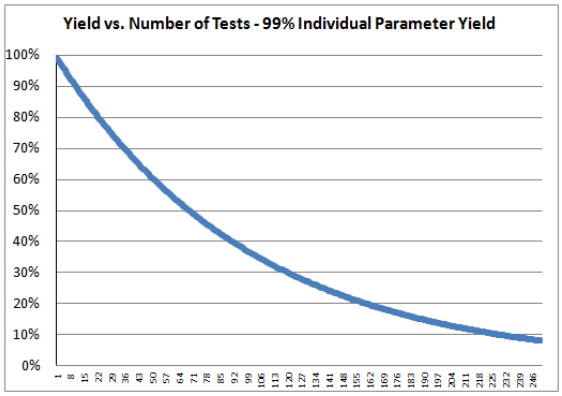


Fig 5: Overall Yield Curve vs. Number of Tests for 99% Exclusive Yield

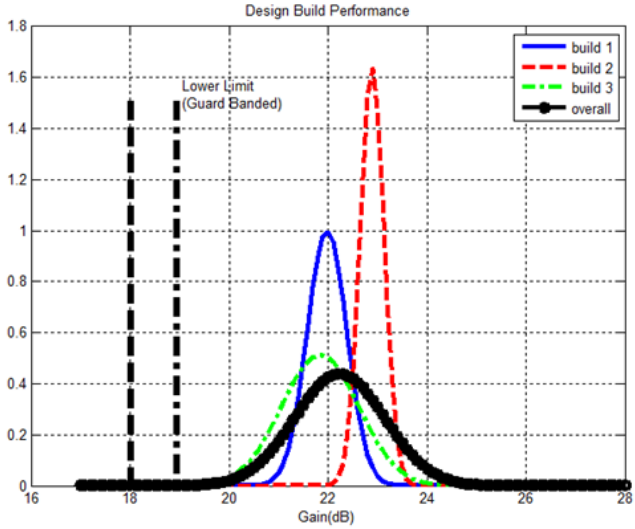
In addition to predicting $\hat{C}_{pk}$, one of the most important activities during product definition is to identify parameters which might not be possible to test reliably (and fast) in mass production. For RFIC modules, such parameters might be Error Vector Magnitude, Noise Figure, Spurious, Leakage. It is important to discuss these parameters in detail early as any parameter(s) which cannot be tested in mass volume must be guaranteed by design.

Proving $\hat{C}_{pk}$ predictions to the design and marketing teams during product definition, based on estimated guard bands and historical variation, helps the teams formulate optimum design targets and datasheet specifications.

III. PLANNING FOR HIGH YIELD DURING DESIGN

During the design phase, first hardware is measured, and engineers are able to begin validating their models and predictions. Mean ($\hat{\mu}$) performance can start to be better understood and improved through design iterations. The difficulty during the design phase is that, because the true product mean is unknown, engineers must make certain assumptions and predictions based on available data. Device performance is influenced by raw materials, fabrication and assembly process, and discrete component variation. Because the entire process is not homogenous, build performance in a given time "snapshot" will not capture longer-term variation and movement of the mean.

For example, during design the mean gain of a power amplifier might be 21.98dB based on ten parts measured from the first design build/spin. Assuming the long-term product mean for this parameters is 21.98dB would be naive. Likewise, the long-term standard deviation will be much larger than the variation of the first ten samples. During each design iteration more and more data becomes available to the engineering teams which allows for better prediction models. Fig 6 illustrates this example, note how the $\hat{C}_{pk}$ is very good for the first two builds, but when we consider more builds and an increased total variation, the overall $\hat{C}_{pk}$ is 1.19.



Build	Mean(dB)	Stdev (dB)	Lower Limit	Upper Limit	Cpk
1	21.98	0.4	19	30	2.48
2	22.89	0.244	19	30	5.31
3	21.84	0.78	19	30	1.21
Overall	22.24	0.91	19	30	1.19

Fig 6: Build $\hat{C}_{pk}$ vs. overall $\hat{C}_{pk}$

During early development, engineers should consider the example shown in Fig 6. Predicting long term yield based on

only a couple of design builds is challenging as knowing the true long term mean and standard deviation is impossible. A pessimistic approach is suggested as the initial build means ***could*** in fact be much ***better*** than the long term mean and variation over time will be much larger than the small initial builds.

Spec negotiation is a critical action during product development. Often, limited data is available for these discussions. The above techniques can be used to minimize yield impact as a result of spec agreements.

IV. PLANNING FOR HIGH YIELD DURING VERIFICATION

Before a design is "locked down" and considered complete, several larger production runs should be built and analyzed. The purpose of these builds should be to capture most of the normal variation of the entire fabrication, assembly, and test process. Corner lots can be used to help better understand the device limitations and impact of critical parameters. There are really two problems with corner lots as they relate to multi-chip RFIC modules: Creating applicable 'corners' might be impossible considering the component interaction, and the New Product Development schedule may not permit extensive 'corners' to be built. Building corner material at the IC die level for a certain parameter might be trivial, but these parameters may not have the biggest impact on the integrated module and the process typically does not drift to the corners. Often building more material to capture the normal process variation of the entire module process is more beneficial than corner lots. However, if known corners exist and the team can create (push) the corners during NPD, this is obviously valuable.

V. IMPROVING YIELD DURING PILOT AND HIGH VOLUME PRODUCTION

Improving yield during pilot production is the next step in the never ending quest for high yields. If the development team has done a good job, a solid foundation should be established when the product launches and high yields should be enjoyed during the pilot phase. Once high yields are established, engineers can spend the majority of their time working on the next development project or looking into special cause events associated with their products.

Pareto charts are used to identify yield inhibitors. Due to the interdependent nature of RFIC multi-chip modules, pareto items may be a result of interactions between many components. As an example, RFIC module gain may be influenced by input matching, PA die, output matching, filter loss, etc. Device binning can be used to "bin out" devices of a desired performance for analysis. It is suggested that devices with excessive values are used for this analysis. P.D. Shainin et. al. [2] refers to these units as the "best of the best" (BOB) and "worst of the worst" (WOW). Engineers compare BOB and WOW devices using many techniques including: electrical analysis, 2D and 3D x-rays, individual component probing and characterization, mechanical analysis (die placement, wire bonds, component placement), SMD measurements, and laminate measurements. Engineers are encouraged to "leave no stone unturned" when it comes to yield analysis and improvement. Fig 7 shows one real-world example where the development engineer found that the largest source of variation for their product came from across laminate panel variation. Through BOB and WOW analysis, cross sections, and 3D x-ray, engineers were able to isolate yield fallout to this laminate variation, with the edges of the panel having more variation and higher means than the center areas.

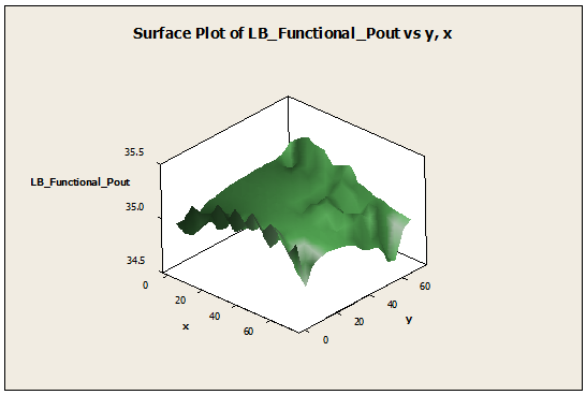


Fig 7: Power out vs. laminate panel location

Fig 8 shows an example of laminate trace measurement for an output tuning element. By comparing BOB and WOW devices, engineers found differences in this turning element and were able to work with the laminate vendor to better control variation in this area.

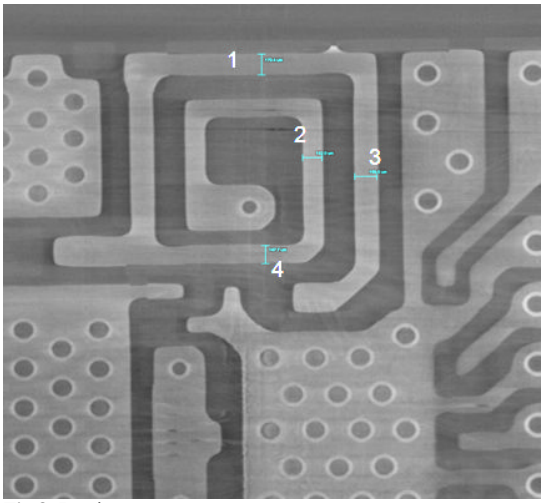


Fig 8: Laminate trace measurements

During volume production, correlations can be established linking overall device parametric performance to other sub component performance and interactions. Establishing correlations with multi-chip modules is challenging as data from certain sub components (e.g. SMDs, Laminates) may not be available as the vendors of these components may not supply this level information. A BOB and WOW analysis can be conducted on a larger population to help understand interdependent correlations related to some of these

components. A. Choo & T. Saeger's paper [3] entitled "Data Analysis for Yield Improvement using TIBCO's Spotfire Data Analysis Software" provides many data analysis techniques which can be used during the production phase of NPD.

VI. CONCLUSIONS

Yield is often the largest lever in terms of product profitability. Considering the huge volume of cellular phone RFIC multi-chip modules, even a 1% yield loss for a high volume product could amount to over half a million dollars in scrap over a few month period. In a low margin, high volume market, every percentage point counts.

Many general techniques were presented within this analysis which should aid the development team during New Product Development. Early prediction is a difficult but required task which can be accomplished using historical data applied to design targets. During design, first articles and additional builds provide empirical data to help optimize yield models. As the design teams get close to finalizing the design, larger builds help validate yield assumptions and set spec limits. Through comprehensive planning, validation, analysis, and specification definition, high yields can often become a reality.

Many articles suggest various areas of NPD activities are "at the center" of solving yield issues (e.g. simulation, characterization, corner lot analysis, etc.) This paper suggests that creating a ***high yield culture*** is really the most critical piece of the entire equation. In order to be successful at launching high yielding volume products, teams need committed, functional members who feel they are a major part of the development team. Additionally, Senior Management should expect nothing less than high yields from these teams. Achieving this cultural shift is the demanding part as engineering teams often think more about technical improvements rather than organizational and cultural enrichment.

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ACRONYMS

BOB: "Best of Best"
Cpk: Process Capability
GaAs: Gallium Arsenide
LSL: Lower Spec Limit
NPD: New Product Development
pHEMT: pseudomorphic High Electron Mobility Transistor
RFIC: Radio Frequency Integrated Circuit
SAW: Surface Acoustic Wave
USL: Upper Spec Limit
WOW: "Worst of Worst"