GaN on Si HEMT Process Transfer and Qualification

John Bell[1], Jeannette James[1], John Kearney[1], Brad Krongard[1], Tom Lepkowski[1], Pradeep Rajagopal[1], Brook Raymond[1*], James Shen[1], Keith Will[1], Chung-hsu Chen[2], Minkar Chen[2], Daniel Hou[2], Chuanxin Lian[2], Libo Song[2], William Sutton[2], Alex Vigo[2], Chao Wang[2], David Wang[2], Shiguang Wang[2]

[1] Nitronex Corporation, 2305 Presidential Drive, Durham NC 27703

[2] Global Communication Semiconductors, Inc., 23155 Kashiwa Court, Torrance, CA 90505

***Phone: (919) 424-5180, Email: braymond@nitronex.com**

Keywords: GaN-on-Silicon, HEMT, AlGaN/GaN, HTOL, Nitronex, GCS

Abstract

Nitronex pioneered AlGaN/GaN HEMTs on commercially available 100mm high resistivity Silicon substrates. Since demonstrating the reliability of the Nitronex NRF1 process technology in 2006, well over 500,000 units have been shipped worldwide to top tier customers. Nitronex has further advanced the manufacturability of AlGaN/GaN HEMTs by successfully transferring the wafer fabrication process to Global Communication Semiconductors, Inc. (GCS). This move increases operational excellence in manufacturability of Nitronex products, utilizing GCS' strengths as a pure-play foundry with their state-of-art dual thread process platform. This paper will discuss the detailed plans and process transfer execution between these two fabs and the resultant qualification studies.

INTRODUCTION

The AlGaN/GaN high electron mobility transistor (HEMT) is ideal for efficient RF high power, multi-octave wide-band applications because of its high power density and high voltage operation. Typical devices produce contact resistance of 0.35ohm-mm, channel sheet resistance of 490ohm/square, maximum channel current of 830mA/mm, peak transconductance of 290mS/mm, drain-gate breakdown >100 volts, Saturated RF Power of 3.9W/mm and maximum drain efficiency of 57% at 28V and 2.14GHz.

NITRONEX TRANSFER PRE-PLANNING

Nitronex developed a three phase transfer strategy comprised of process module development, integration and qualification. The philosophy comprised of copying Nitronex key process modules and re-use GCS existing processes for others when possible. This philosophy added some risks over the more conservative copy exact method, but avoided the significantly higher costs associated with supporting additional potentially redundant equipment and lost opportunity to take advantage of more automated dual thread tool sets at GCS. The complexity of Nitronex NRF1 AlGaN/GaN HEMT process platform was divided into several module levels. The break points between modules were selected to minimize interactions with other modules. This allowed the critical outputs of each module to be treated independently from other modules during the first phase of the transfer process. Nitronex methodically examined the critical aspects every process to establish a comprehensive list of tangible requirements necessary to qualify the process. These requirements included equipment process parameters, in-line monitoring, device and test data, such as temperature, thickness, refractive index, CD, misalignment and slope. Where module requirements included an electrical performance assessment, the plan included process lots. Usually processing of Module Lots consisted of mostly Nitronex baseline modules with the evaluation module processed at GCS. The Integration phase consisted of several lots processed solely at GCS staggered over time to evaluate performance of GCS' newly developed process and comparison against requirements. The Qualification phase included packaged part performance using Nitronex standard suite of Reliability tests, including temperature cycling, ESD and HTOL (High Temperature Operational Life Test.)

TRANSFER TEAM PLANNING

In October 2009 planning of the transfer stages and criteria were finalized. The GCS Team visited the Nitronex facility for initial briefing and tour of the Nitronex facility. At this time a great deal of collaboration occurred between the two Teams. The Nitronex processes and equipment were described in detail to the GCS Team, and the GCS process and equipment capabilities were described to the Nitronex Team. Both Teams considered the requirements and any potential differences between the two fab processes as they mapped each individual process from the Nitronex fab into each similarly functioning process tool at the GCS fab. Critical off-line measurement techniques were also compared and treated in the same manner as process steps. GCS provided feedback when significant differences existed in equipment or process capability which led to an optimized

implementation strategy. From this collaborative effort the plan was refined and formalized. A risk assessment of this plan was performed to mitigate these risks. The three high risk areas identified were lack of a dedicated RTA, a high voltage SMU and a Sputter system with Titanium capability. To address these risks, Nitronex and GCS entered a cost sharing agreement to purchase necessary equipment. Facilitating these additional tools required GCS to expand their clean room area. In addition GCS expanded other resources including technical staff and fab shifts per week. The two medium risk areas identified were the PECVD Silicon Nitride Deposition tool and photolithography materials. GCS had a similar PECVD development tool but production experience favored an automated load-locked Novellus tool. GCS had production experience with numerous photoresists, but did not have specific production experience with negative tone photoresist. In both of these cases the ability to copy exact was available but the opportunity to adopt GCS' existing technology provided compelling justification to change. Since copy exact remained a viable backup alternative, these risks were demoted. A great deal of effort went into this transfer project affecting many different processes. In the remaining portion of this paper, we will not attempt to explore details of every aspect of this process transfer; instead the discussion will focus attention to areas involving technical challenges in the critical path to success.

MODULE TRANSFER PHASE

During module development, Nitronex staff frequently visited the GCS fab to assist in process development. Emphasis was placed on developing front-end modules first due to the additional process time necessary to complete fabrication at Nitronex. Evaluation lots for latter back-end modules were fabricated at Nitronex ahead of schedule and then staged in anticipation of GCS module development effort.

Unfortunately two setbacks during front-end processing occurred. First was an unexpected supplier delay in receiving the RTA equipment. Second was a failure of the initial Novellus PECVD film to meet all requirements. This PECVD film had numerous stringent requirements, as it was known by Nitronex to be critical for device DC and RF performance. An especially difficult constraint placed on GCS' Novellus development was the avoidance of LF RF typically used on this tool to reduce the film's tendency toward higher tensile stress. Equipment modifications were necessary, primarily involving additional gasses. With that change came extensive process development work necessary to dial in the reactor process to simultaneous achieve all requirements, notably BOE etch rate, film stress and refractive index. Once the GCS developed film matched properties of the Nitronex film, a Nitronex Lot was split with half receiving GCS' passivation. DC and RF (figure 1) characterization confirmed that device performance was unchanged with this new film.

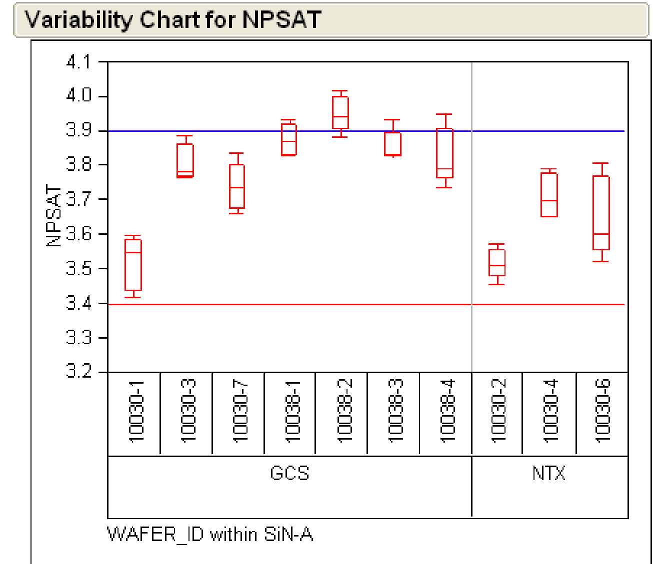

Figure 1. Normalize saturated RF power by Fab Passivation

Once these struggles were resolved the module lots were completed with very few complications. It took roughly 7 months and approximately 100 wafers processed at GCS, to successfully qualify the Module phase.

INTEGRATION PHASE

As per the plan, the Integration lots were processed solely at GCS. Another setback occurred just as the lead integration lot completed FET PCM testing. A serious reverse leakage current problem became apparent. Trends of leakage current (Figure 2) including earlier successful module data provided statistical clues that focused attention on the Ohmic Module.

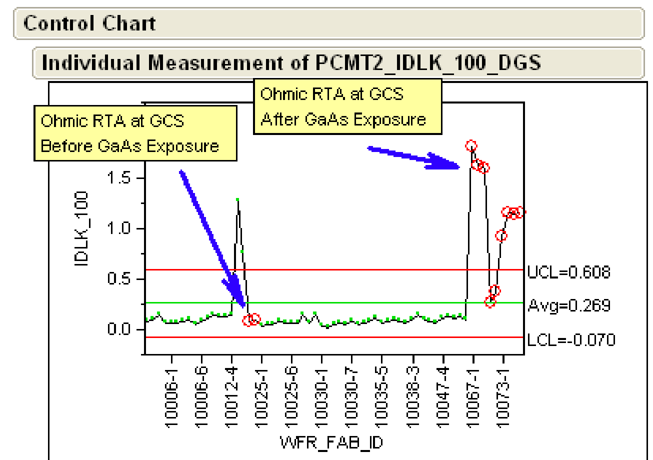

Figure 2. Mean wafer leakage trend, GCS (circle), Nitronex (dot)

This was an unusual clue, since gate leakage had never been attributed to interactions with the Ohmic module at Nitronex. Integration lots were suspended prior to the Ohmic module pending resolution. A three factor DOE lot was constructed to confirm initial suspicions.

Effect Tests

Source	Nparm	DF	Sum of Squares	F Ratio	Prob > F
GCS Ohmic Descum	1	1	0.6329278	35.4914	0.0040
GCS Ohmic Anneal	1	1	1.4776481	82.8590	0.0008
GCS SiNA	1	1	0.1544693	8.6619	0.0423

Table 1. Ohmic DOE Leakage Current Effects by Process Step

Based on the DOE results (Table 1), the RTA tool was scrutinized. Small differences in alloy appearance provided important insight. These subtle metallurgical differences between the two fabs (Figure 3) became a leading indicator of leakage performance.

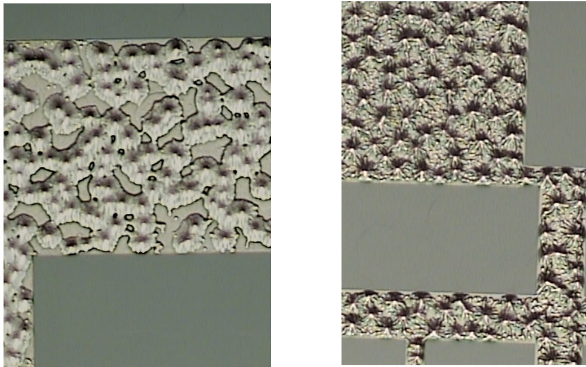

Figure 3. Typical (left), abnormal (right) Post Alloy Morphology

Because GCS' fab produces GaAs devices, one suspect was arsenic contamination. Log sheets confirmed that the first GaAs wafer processed on this RTA ran after the last good GaN wafer had been processed. Once the tool was fitted with a new chamber and susceptor, the alloy appearance returned to normal. The DOE also showed that the Descum process also impacted leakage currents. Once the Nitronex Descum recipe was copied to the GCS tool, leakage current returned the expected range. Based on these findings, usage restrictions were adopted for the RTA to prevent future occurrences.

Once the Ohmic problems were corrected, processing resumed without issue. Following Integration Lots met Nitronex requirements. The early problem detection and ultimate success during the Integration Phase allowed us to use most of the Integration Lots in the final Qualification phase.

QUALIFICATION PHASE

The Qualification Phase kicked off 14 months after the fab transfer first initiated. As per plan, specification compliant wafers from three different Integration or Qualification lots were selected for this task. KGD testing and inking was performed on completely processed wafers at GCS. The die selected for use as the qualification vehicle was based on our high running product line's 25W device housed in ceramic a package (NPTB00025.) All post fab assembly and test activities followed qualified Nitronex procedures. Two hundred GCS Qualification devices were compared to random sampling of Nitronex Production Devices from a mix several lots (Figure 4 and 5.) No deficiencies between GCS and Nitronex fabricated devices were observed.

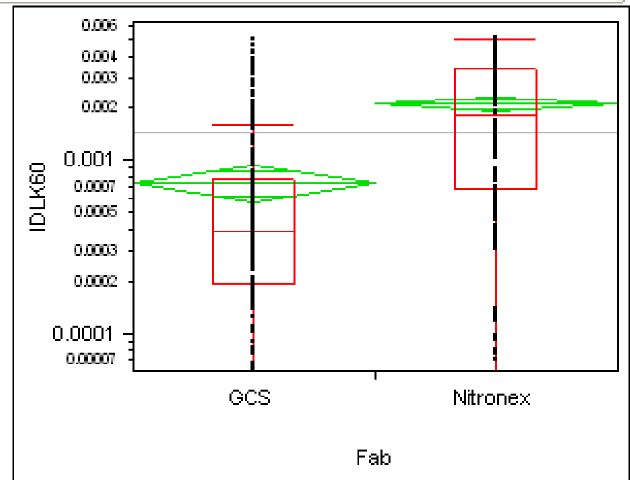

Figure 4. NPTB00025 Leakage Current by Fab

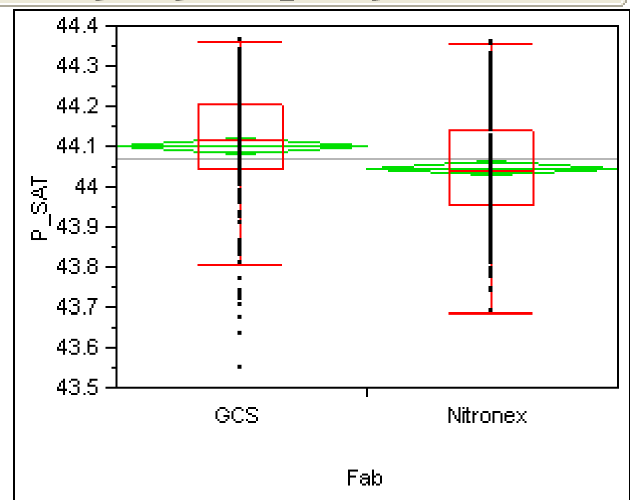

Figure 5. NPTB00025 Saturated RF Power by Fab

GCS fabricated devices were used to demonstrate reliability to Nitronex standards based on industry accepted Military Standard 883 and JESD22. For HTOL this demanded a quantity of 106 GCS devices stressed at a maximum junction temperature of 200ºC for 1000 hours with a drain voltage of 28V. These reliability tests are summarized in Table 2.

Test Name	Test Standard	Sample Set	Status
HTOL	JESD22-A108	106 devices, 1000 hours	Complete, passed
TC	JESD22-A104	45	Complete, passed
BS	Mil-Std-883 Method 2011	15	Complete, passed
ESD-HBM	JESD22-A114	3	Complete, passed Class 1A (>250V)
ESD-CDM	JESD22-C101	3	Complete, passed Class IV (>1000V)

Table 2. Status of GCS Device Reliability Test

CONCLUSIONS

The successful Process Qualification of GaN on Silicon HEMT's at GCS required 17 months of coordinated collaboration and dedication from personnel at both companies. Understanding the underlying critical characteristics proved essential to achieving first pass success. Experienced engineers made light work of matching these characteristics to different tool sets. Some previously unknown interactions were discovered along this path, related to intermixing GaN and GaAs fabrication processes and new controls were established. Careful planning enabled the use of comparative analytics to a referenced stable process which played an essential role in identifying and correcting specific problems. By adopting a flexible transfer strategy, Nitronex can now realize the more automated and capable suite of GCS process tools.

ACKNOWLEDGEMENTS

Many individuals contributed significant time and effort to make this transfer successful. Special thanks goes to technicians from both company's working days, nights and weekends with great skill to process numerous wafers necessary for success.

ACRONYMS

BS: Bond Strength
CD: Critical Dimension
CDM: Charged Body Model
DC: Direct Current
DOE: Design of Experiment
ESD: Electro-Static Discharge
FAB: Fabrication Facility
FET: Field Effect Transistor
GaAs: Gallium Arsenide
GCS: Global Communication Semiconductors
HEMT: High Electron Mobility Transistor
HTOL: High Temperature Operating Life
HBM: Human Body Model
IDLK: Reverse-bias Gate-to-Drain Leakage Current
JEDEC: Joint Electron Device Engineering Council
JESD: Joint Electron Standards and Documents
KGD: Known Good Die
LF: Low Frequency
NPSAT: Normalized Saturated RF Power
NTX: Nitronex
PECVD: Plasma Enhanced Chemical Vapor Deposition
PCM: Process Control Monitor
RF: Radio Frequency
RTA: Rapid Thermal Anneal
SIN-A: First Silicon Nitride Passivation Layer
SMU: Source Measurement Unit
TC: Temperature Cycling