

# Novel Passivation Ledge Monitor in an InGaP HBT Process

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## Abstract

**The HBT ledge thickness and quality is vital for device performance and reliability. In this work we report on a measurement technique and test structure for monitoring the emitter passivation ledge based on the use of TaN as a barrier between the InGaP ledge surface and the top metal contact. The technique is suitable for the manufacturing environment.**

## INTRODUCTION

InGaP/GaAs heterojunction bipolar transistors (HBT) are widely used for wireless applications since they have excellent features such as high power density and high efficiency. The performance and reliability of the HBT is greatly influenced by the effectiveness of the emitter ledge [1-3]. This ledge reduces the recombination current providing better device scaling and improved reliability.

Given the importance of the HBT ledge thickness and quality, monitoring these allows for better in-line control and wafer screening. Previously, in an AlGaAs HBT process, a ledge monitor was successfully demonstrated by using the first interconnect metal layer as the top electrode [4, 5]. The metal layer, a Ti/Pt/Au stack, was deposited directly on the AlGaAs passivation ledge to form a metal insulator semiconductor (MIS) capacitor between M1 and the HBT p+ base. In-line capacitance measurements of this structure allowed for the monitoring of the ledge thickness and quality. Moreover, by using such a contact, a guard-ring on the HBT ledge, and monitoring the potential of this contact during a Gummel measurement, one can distinguish between pinched and un-pinched ledges and to determine the passivation quality [4].

However, if the emitter is changed from AlGaAs to InGaP, this original structure no longer functions correctly. To our knowledge, there are currently no simple in-line electrical tests to monitor ledges in an InGaP HBT process. In this work we propose the use of TaN as a barrier that allows us to develop the test structure to monitor the InGaP passivation ledge.

## CONVENTIONAL METHOD

The use of Schottky contacts on InGaP/GaAs heterostructures is ubiquitous in the gate definition of

pHEMT and FET devices since the n-type InGaP layer acts as an etch-stop layer and it has high energy band-gap. Contact stacks of Ti/Pt/Au are used routinely in production with excellent low gate leakage current and high gate breakdown voltage.

Given the omnipresence of such metal stacks as InGaP contacts, one would think that its use on an HBT ledge is appropriate. However, there is a major difference between the two cases. Although the n-type InGaP layer thickness is similar in both cases, the layer adjacent to the InGaP is a highly doped p++ GaAs base instead of the AlGaAs or n-doped GaAs used for FETs or HEMTs channels. The result is a structure with two diodes in opposite direction, one Schottky and one heterojunction compared with just a Schottky diode in the common case.

Our attempts to use our standard first metal interconnect, a Ti/Pt/Au stack, to form the InGaP Schottky contact resulted in high resistivity ohmic contacts making characterization of the InGaP layer difficult. We believe using the Ti/Pt/Au stack forms a degraded version of the base ohmic contact shown in [6].

## WHY TAN?

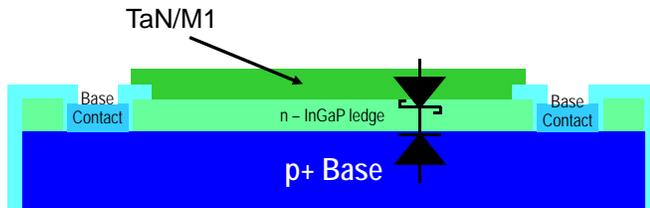
The use of TaN as a barrier is well known in the silicon world. There they employ barrier layers such as Ta, TaN, TaSiN, TiN, and WN. Among these, TaN is the most effective [7], due to its high thermal stability, low resistivity, and low diffusion constants. In GaAs processes, TaN films do not show intermixing with GaAs even after annealing at 550 °C, and display very sharp interfaces [8]. In addition, TaN is also compatible and available in our current InGaP process since it is used as the material layer for precision thin-film resistors.

## DEVICE STRUCTURE AND TEST RESULTS

The devices used in this work were fabricated using the standard Skyworks InGaP HBT process. To explore the characteristics of this structure we fabricated devices of various sizes. Smaller devices with TaN area between  $1 \mu\text{m}^2$  and  $100 \mu\text{m}^2$  were used to characterize the DC operation, while large devices were used for capacitance measurements. In the latter case, to make fringing

capacitance effects negligible, devices of  $3600 \mu\text{m}^2$  were used.

The fabrication process involves the deposition of a TaN layer on top of the HBT ledge following the emitter mesa definition. Subsequent steps require the base pedestal formation and the layout of the base contact. The device can be tested after the first metal interconnect which is deposited to contact both the TaN and base contact terminals of the device. A schematic of the device cross-section is presented in Figure 1.



**Figure 1. Schematic of the ledge diode.**

An ideal TaN contact on the n-doped InGaP layer will form a Schottky diode where the TaN layer will become the anode. The InGaP layer and the highly p-doped base is a heterojunction where the base is the anode. The resulting structure thus has two diodes in the opposite direction.

Since the doping concentration of the HBT base is much higher than the doping concentration of the InGaP ledge, the heterojunction is, in effect, a one-sided abrupt junction. Thus, the depletion region in the base layer is negligible while the depletion layer in the InGaP can be estimated then by the simple expression at equilibrium:

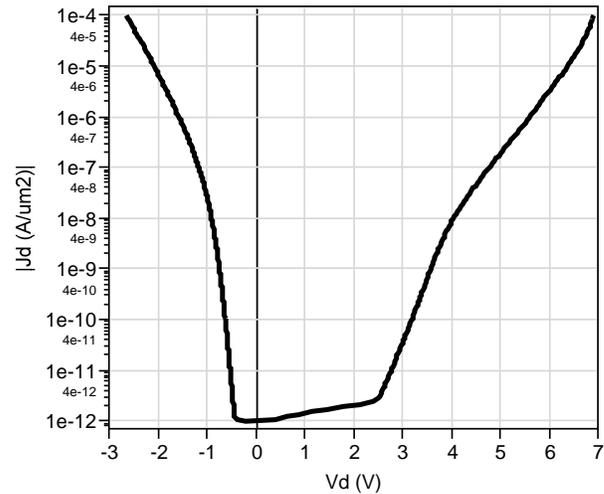
$$W \cong \sqrt{\frac{2\epsilon V_{bi}}{qN_D}}, \quad (\text{Eq. 1})$$

which in our case yields a dimension of more than  $800 \text{ \AA}$ , larger than the ledge thicknesses considered in this study.

Similarly, looking from the TaN side, the Schottky diode depletion width is approximately  $600 \text{ \AA}$  for a built-in voltage of about  $0.5 \text{ V}$ . Based on these considerations, the device is a metal-insulator-semiconductor (MIS) tunnel diode at equilibrium, although the insulator, in this case the InGaP, has a bandgap of only  $1.9 \text{ V}$ .

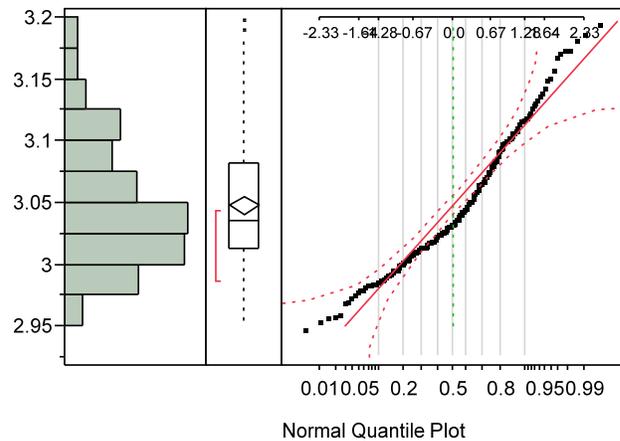
The resulting DC operation of the device is depicted in Figure 2. The figure shows a typical I-V characteristic of the new device. In the picture, the voltage is applied to the TaN terminal. When positive bias is applied to the TaN terminal, the current is limited by the reverse diode current of the heterojunction and not by the TaN Schottky turn-on voltage. The breakdown voltage of the heterojunction is determined to be approximately  $5 \text{ V}$  at a current density of  $0.1 \mu\text{A}/\mu\text{m}^2$ . The TaN Schottky diode has a measured barrier height of approximately  $0.5 \text{ V}$ . When negative bias is applied to the TaN terminal, the device will behave ohmic above the lower

TaN barrier height, or similar to a forward-biased heterojunction with a lowered turn-on voltage.



**Figure 2. Forward and reverse I-V curve of the TaN ledge diode (absolute value, diode area of  $90 \mu\text{m}^2$ ).**

Variations in the I-V characteristics of the structure can give information on the ledge thickness and quality. However, since the InGaP layer is fully depleted at equilibrium, measuring capacitance without bias is much more practical since it allows a fast, reliable, and automated test method. For this purpose we used the large area device of  $3600 \mu\text{m}^2$  which is tested in-line, as part of the process control module testing. The large capacitance makes it easy to test using common LCR meters at lower frequencies of  $1 \text{ MHz}$ , with high precision and accuracy. The device yields a capacitance in the range of  $11 \text{ pF}$ , or a capacitance density of approximately  $3 \text{ fF}/\mu\text{m}^2$ . Figure 3 shows the capacitance density distribution as measured across a wafer lot.

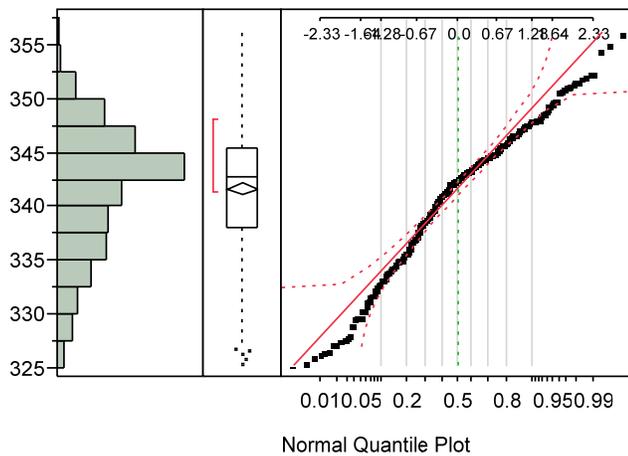


**Figure 3. Distribution of measured ledge capacitance density ( $\text{fF}/\mu\text{m}^2$ ) across a wafer lot.**

Using the simple capacitance relationship:

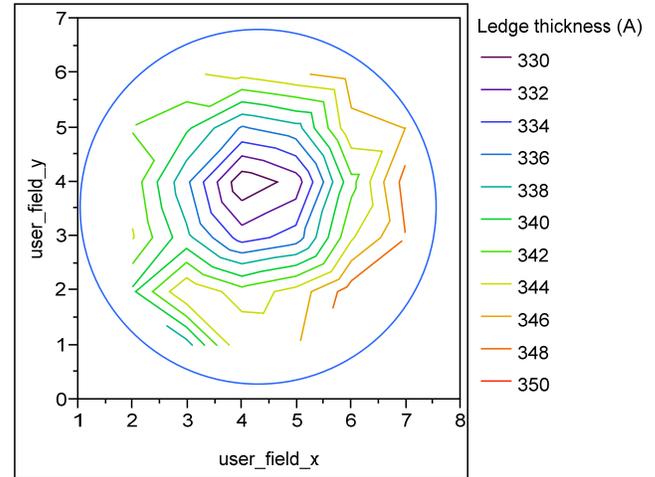
$$C = \frac{\epsilon_r \epsilon_0 A}{d}, \quad (\text{Eq. 2})$$

we calculate the InGaP ledge thickness by using a value of 11.75 for the InGaP relative permittivity. Figure 4 shows that the average ledge thickness for this sample is 340 Å, while Figure 5 shows the average ledge thickness distribution across the wafers. The results across multiple lots show consistently that the variation of the ledge thickness across wafers is less than 30 Å.



**Figure 4. Distribution of calculated ledge thickness (Å) across a wafer lot.**

We can further investigate the accuracy of the ledge thickness measurement method by looking at the expected variations from the parameters that determine the ledge. First, the area of the device has a variation induced by the TaN sizing variation. In the current process, a maximum deviation of 0.4 μm can be considered, which results in a device size variation of up to 1.3%. In addition, the capacitance measurement equipment has a listed accuracy of less than 0.1% for our capacitance range and frequency. Since the test accuracy is much better than the expected variation from the TaN process, we consider only the latter to conclude that our ledge thickness measurement has an accuracy of less than 5 Å.



**Figure 5. Averaged ledge thickness variation across wafers.**

## CONCLUSIONS

In conclusion, with this work we report on a measurement technique and test structure for monitoring the emitter passivation ledge based on the use of TaN as a barrier between the InGaP ledge surface and the top metal contact. The test structure forms a metal-insulator-semiconductor device which yields precise capacitance measurements. Based on these measurements we can determine the ledge thickness with high accuracy. Thus, the technique is suitable for the manufacturing environment to assess the passivation ledge thickness and quality. This technique can also serve as early screen for potential reliability or process related device degradation.

## ACKNOWLEDGEMENTS

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#### ACRONYMS

HBT: Heterojunction Bipolar Transistor

pHEMT: pseudomorphic High Electron Mobility Transistor