Dry Wide Recess Process Characterization for PHEMT

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Abstract

The manufacturing capacity of PHEMT devices needed to be increased in order to meet higher demand. A new dry plasma etch platform, SPTS CPX, was brought in for this purpose. The objective of this study was to characterize the dry wide recess process for PHEMT on the SPTS prior to release for production. The experiment was set up by creating a screening design of experiment (DOE), then a full factorial DOE. Results from the screening DOE identified an unstable region in the process space. This allowed the full factorial DOE to be designed to avoid the unstable region in the process space. Analysis of the DOE results indicated an area of process space which could potentially be used for the production of PHEMT devices.

INTRODUCTION

The dry wide recess etch process requires a plasma platform capable of low bias power and low pressures; it targets removal of the GaAs layer and stops on AlGaAs. The etch rate requirements are in Table I and a cross section of the dry wide recess is shown in Figure 1. Plasma ion damage to the AlGaAs layer must also be minimized to ensure good gate performance. A process running with lower bias power has less ion energy which limits ion damage. The SPTS CPX, a new plasma etch platform was installed for this purpose - to increase manufacturing productivity for PHEMT devices and replace older equipment. This process currently runs on PMT Pinnacle and Renaissance tools, both using a MORI source for its plasma. The SPTS CPX platform uses an ICP source located closer to the wafer than the MORI source bell-jar. The new platform with its inherent differences required thorough characterization of the dry wide recess process using DOE methodology prior to production use.

TABLE I
ETCH REQUIREMENTS

Etch Requirements	Target
GaAs removal	1200A
AlGaAs removal	< 50A
Oxide mask erosion	< 200A

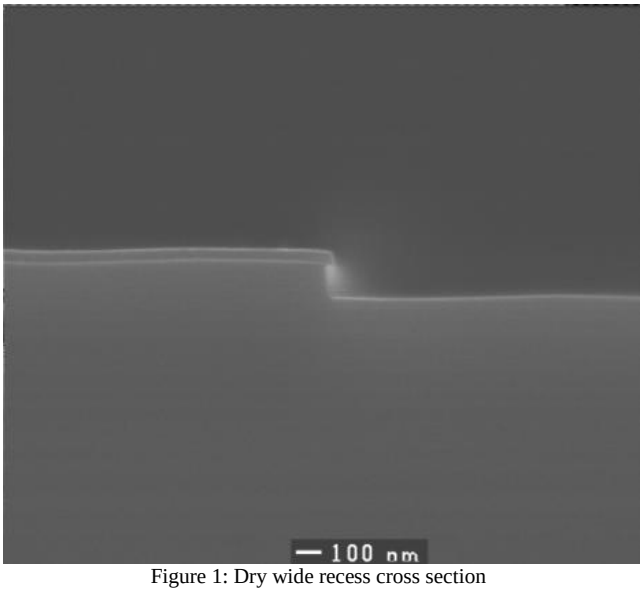

Figure 1: Dry wide recess cross section

CHARACTERIZATION PROCEDURE

The dry wide recess process targets the removal of GaAs, therefore, it was crucial that a consistent type of GaAs wafer be used for the experiment. Etch rate tests were set up by using a known dry wide recess process to determine the wafer type that gave the most accurate results. Then the characterization procedure was set up in two parts. First, a screening DOE was set up to gain insight into the general process behavior of the SPTS CPX over a wide range of process conditions. Then, based on the screening DOE, a full factorial DOE was created for the appropriate process space to fully characterize the dry wide recess process on the SPTS CPX for PHEMT.

WAFER TYPE

The etch rate data was obtained by building a test wafer structure with the same oxide hard mask as product and using only GaAs material below the oxide hard mask. Wafers were etched and then the etching depth was measured using a Tencor Profilometer.

Initial etch rate measurement results using bulk GaAs mechanical wafers showed a rather strange behavior, where the etch rate stayed nearly constant with time. After researching the sources for GaAs test wafers it was discovered that some test wafers were actually rejected GaAs wafers with epi layers under the GaAs. These wafers were repurposed as test wafers, but the epi films blocked the process from etching further, causing the abnormal etch rate. The virgin GaAs wafer's etch rate results are shown in Figure 2, where the etch rate increases linearly with time. As expected, longer etching time allows the plasma to etch away more material. Therefore, to ensure accuracy of the experiment only virgin GaAs wafers were used.

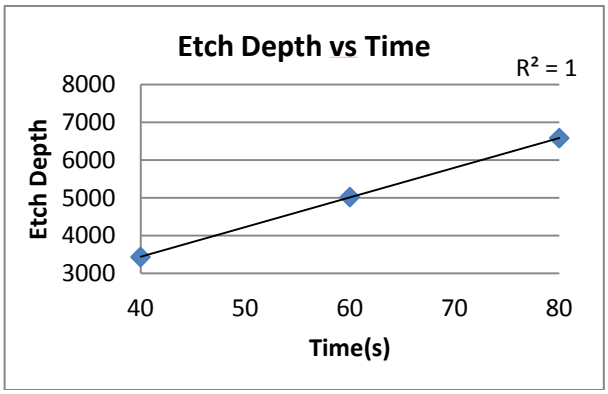

Figure 2: Virgin GaAs etch rate

SCREENING DOE

A screening DOE was created based on the process of record running on the older etch equipment, Table II. The screening DOE samples a portion of the process space to gain an idea of its behavior over a wider range of process conditions. BCl_3 flow was varied from 7 to 10 sccm. The platen and coil powers were varied between 5- 20W and 250 – 450W, respectively. The results indicated the processes sensitivity to bias and coil powers at low BCl_3 flow, resulting in an unusually slow etch, Figure 3. One hypothesis is that there is a reduced amount of heavy Cl containing ions at low BCl_3 flow, and when combined with low bias (reduces ion energy) it can prevent breakthrough of the oxidized surface. Another hypothesis is the BCl_3/SF_6 ratio, experimental results have shown that when higher percentage of SF_6 is present, it inhibits the etch, caused by an increase in formation of gallium fluoride, which would cause the unstable etch[1].

TABLE II
PROCESS OF RECORD

Pressure	Coil Power	Bias Power	BCl3	Time
2.5mTorr	350W	15W	8sccm	30s

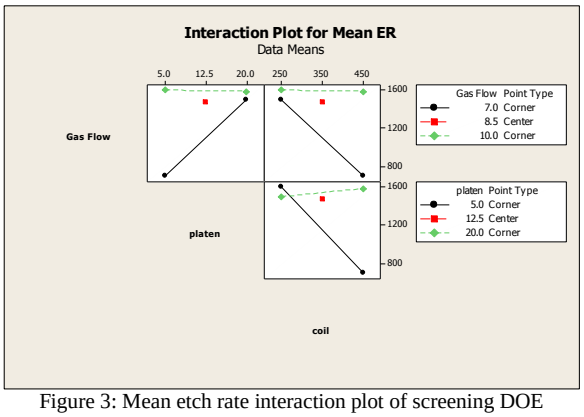

Figure 3: Mean etch rate interaction plot of screening DOE

FULL FACTORIAL DOE

Based on the screening DOE, a full factorial DOE was created to better investigate the optimal region of process space. The BCl_3 flow conditions were changed in order to avoid the abnormally slow etch conditions. At the same time, the GaAs and oxide mask selectivity were investigated. Even with a slightly higher BCl_3 flow, there was still an unusual decrease in etch rate at lower BCl_3 flow and high coil power, likely caused by an increase in percentage of SF_6 as mentioned previously, Figure 4. Therefore, BCl_3 flow at minimum of 9sccm or 10sccm should prevent the etch from the 'falloff' region where the etch decreases dramatically.

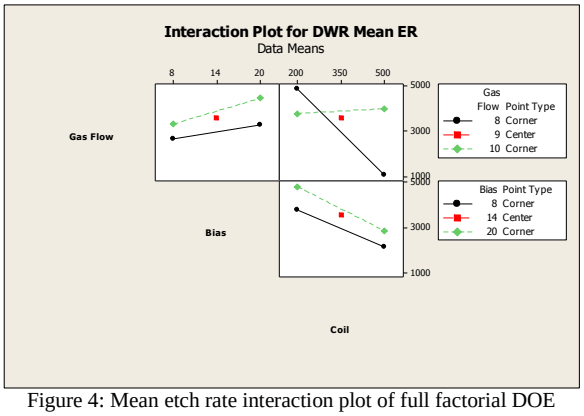

Figure 4: Mean etch rate interaction plot of full factorial DOE

The selectivity of GaAs versus oxide results indicated a significant decrease in selectivity as bias and coil power are increased, Figure 5. This phenomenon can be explained by the increase in ion energies as bias power is increased and increase in ion density / plasma density as coil power is increased. As ion energies and / or densities increase the physical etch component (sputtering) of both the GaAs and the oxide materials also increases, driving down the selectivity ratio. This indicates that when the RF increases, eventually the physical removal of the material can eclipse the chemical removal rate. At lower RF powers, the selectivity was greater because the main etching mechanism

was chemical and the chemistry was designed specifically to react with the GaAs material and form a passivating film on the AlGaAs layer.

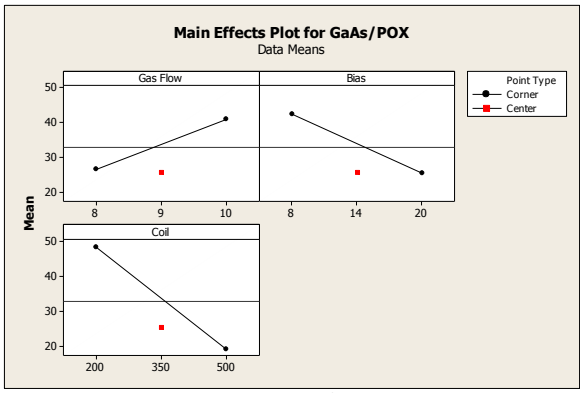

Figure 5: Selectivity of GaAs/Oxide

From the data, the recommended optimum dry wide recess process for the SPTS CPX platform would then be one that runs with BCl_3 at 9 or 10sccm, 12W bias and 300W coil power to reach the target of 1200A GaAs removal and to avoid too much loss of selectivity to the oxide mask layer, Table III.

TABLE III
OPTIMUM DRY WIDE RECESS PROCESS

Pressure	Coil Power	Bias Power	BCl3	Time
2.5mTorr	300W	12W	9-10sccm	20s

CONCLUSION

The dry wide recess process DOE characterization for PHEMT on a new SPTS CPX platform has given insight into the behavior of the process. It has indicated two areas of process space to avoid: low gas flow combined with either low bias power or high coil power. Analysis has shown a set of parameters that could potentially be qualified for production. The next step is to conduct further research to investigate the wafer-to-wafer and lot-to-lot stability, plasma emission endpoint characterization, damage performance and CD performance on the SPTS CPX. These next steps will be necessary to determine the manufacturing capability of PHEMT devices on the SPTS CPX.

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ACRONYMS

DOE: Design of Experiment
PHEMT: Pseudomorphic mobility transistor

REFERENCES

1. Y.-S. Lee, K. Upadhyaya, K. J. Nordheden, and M.-Y. Kao, 2000, Selective reactive ion etching of GaAs/AlAs in BCl3/SF6 for gate recess, *Journal of Vacuum Science and Technology B*, v. 18. doi:10.1116/1.1288134