Removal of Surface-Related Current Slump in Field-Plate GaAs FETs

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Abstract

Two-dimensional transient analysis of field-plate GaAs MESFETs is performed in which surface states are considered. Quasi-pulsed current-voltage curves are derived from the transient characteristics. It is shown that the drain lag and current slump due to surface states can be reduced by introducing a field plate because fixed potential at the field plate leads to reducing trapping effects by the surface states. The dependence of lag phenomena and current slump on field-plate length and SiO_2 passivation layer thickness is also studied, indicating that the lags and current slump can be completely removed in some cases.

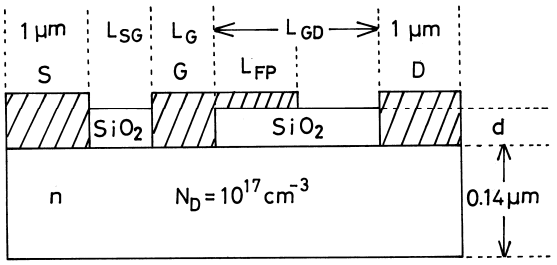

Fig.1 Device structure analyzed in this study.

INTRODUCTION

In compound semiconductor FETs, slow current transients are often observed when the drain voltage or the gate voltage is changed abruptly [1,2]. These slow current transients are called drain lag or gate lag, and are undesirable for circuit applications. The dc and RF current-voltage (*I-V*) curves from devices with gate lag are significantly different, resulting in lower RF power available than would be predicted from dc operation [3]. This difference is called current slump. These phenomena occur due to the presence of surface states and/or bulk traps in the device [1-5]. Experimentally, the introduction of a field plate (Fig.1) is shown to reduce the lags and current slump [3,6,7]. Though some work on GaN-based FETs with bulk traps has been performed [8], few simulation studies on field-plate structures have been published.. Therefore, in this work, we have made a two-dimensional transient simulation of GaAs MESFETs that includes surface states, and found that surface-related lags and current slump can be reduced, or in some cases completely eliminated, by introducing a field plate [9].

PHYSICAL MODELS

Fig.1 shows a device structure analyzed in this study. The gate length L_G is typically set to 0.3 μm. The gate electrode extends onto the SiO_2 passivation layer. This extension is called a field plate. This paper examines the effect of field plate length L_{FP} and passivation layer thickness d on device performance. In order to increase the model accuracy, surface states are usually considered on the planes between the source and the gate and on the planes between the gate and the drain. In some cases, relatively large densities of surface states are considered only at the drain edge of the gate region. This situation can occur after the device has been stressed or due to device degradation. As a surface-state model, we adopt Spicer's unified defect model, and assume that the surface states consist of a pair of a deep donor and a deep acceptor. The surface states are assumed to distributed uniformly within 5Å of the surface, and their densities (N_{SD}, N_{DA}) are typically set to $2.5\text{x}10^{19}$ cm^{-3} ($1.25\text{x}10^{12}$ cm^{-2}), but they are varied between $2.5\text{x}10^{19}$ cm^{-3} ($1.25\text{x}10^{12}$ cm^{-2}) and $6\text{x}10^{19}$ cm^{-3} ($3\text{x}10^{12}$ cm^{-2}). The energy levels of the surface states used in the model were based on previously published experimental work [10]: E_{SD} = 0.87 eV, E_{SA} = 0.7 eV, where E_{SD} is the energy difference between the bottom of conduction band and the deep donor's energy level, and E_{SA} is the energy difference between the deep acceptor's energy level and the top of valence band. In this case, the deep-acceptor surface state mainly determines the surface Fermi level, and acts as a hole trap.

The model is based on Poisson's equation (including ionized deep-level terms), continuity equations for electrons and holes which include carrier loss rates via the deep levels, and rate equations for the deep levels [9-11]. These equations are put into discrete form, and solved numerically. The model calculates the drain-current responses when the drain voltage V_D and/or the gate voltage V_G are changed abruptly.

SLOW CURRENT TRANSIENTS

Fig.2 shows calculated drain-current responses of GaAs MESFETs considering surface states when V_D is lowered abruptly from 10 V to V_{Dfin}, where V_G is kept constant at 0 V. Here, the surface-state density is $1.25\text{x}10^{12}$ cm^{-2}, and surface

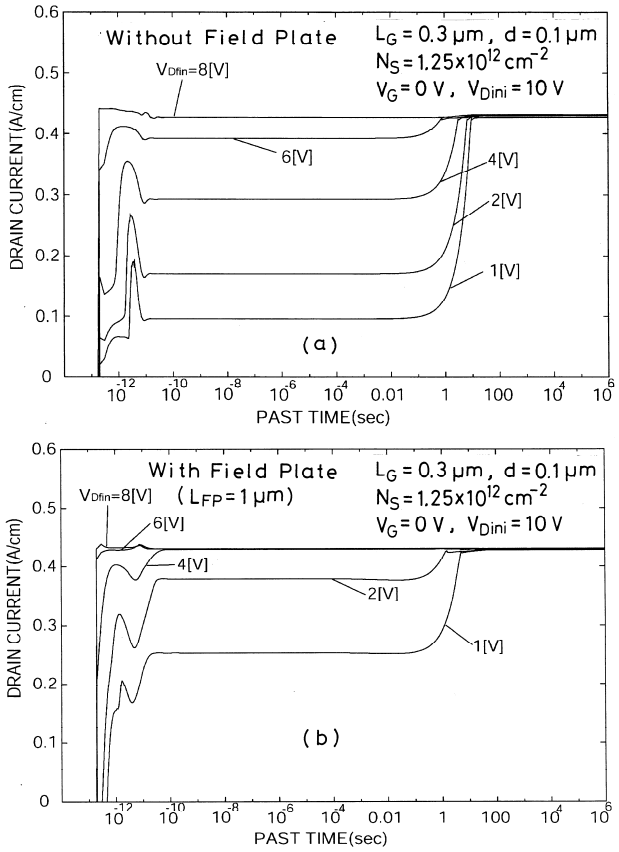

Fig.2 Calculated drain-current responses of GaAs MESFETs with surface states when V_D is lowered abruptly from 10 V to V_{Dfin}, while V_G is kept constant at 0 V. N_S = 1.25x10^{12} cm^{-2}. (a) Without field plate, (b) with field plate (L_{FP} = 1 μm, d = 0.1 μm).

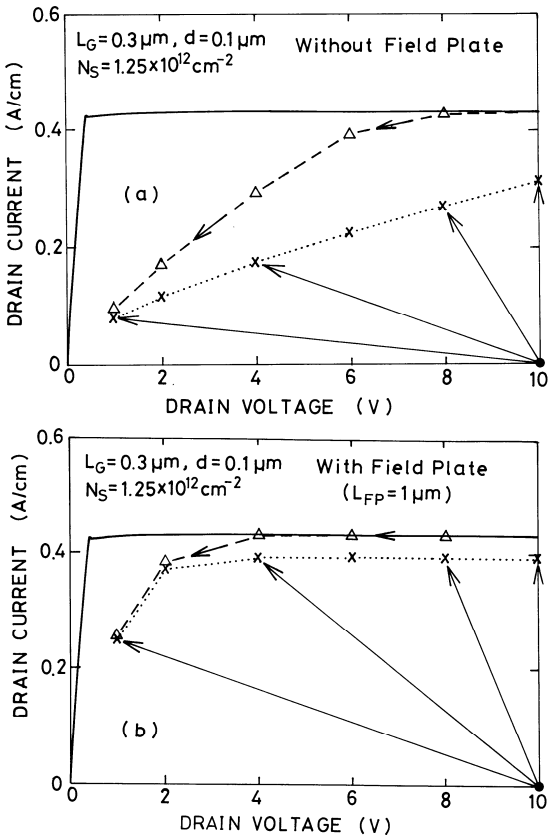

Fig.3 Steady-state I-V curves (V_G =0 V; solid lines) and quasi-pulsed I-V curves (Δ, x) of GaAs MESFETs with surface states. N_S = 1.25x10^{12} cm^{-2}. (a) Without field plate, (b) with 1 μm-length field plate. d = 0.1 μm. (Δ): Only V_D is changed from 10 V (t = 10^{-8} sec), (x): V_D is lowered from 10 V and V_G is changed from V_{th} to 0 V (t = 10^{-8} sec).

states are considered along the entire region between source and gate and between gate and drain. Fig.2(a) shows a case without a field plate, and Fig.2(b) shows a case with a field plate (L_{FP} = 1 μm). The thickness of SiO_2 layer d is 0.1 μm. In both cases, the drain currents remain at low values for some period (10^{-10} – 10^{-1} s) and then begins to increase slowly, showing drain lag behavior. It is understood that the drain currents begin to increase when the deep-acceptor surface states begin to capture holes [11] or emit electrons. It is clearly seen that the change of drain current is smaller for the case with a field plate when comparing at the same V_{Dfin}, indicating that the drain lag is smaller for the field-plate structure. Without the field plate, a barrier for electrons is formed at the gate-to-drain region during the transients, and hence I_D becomes very low. On the other hand, with a field plate, the potential under the field plate is almost flat and a small barrier is seen between the field plate and the drain, and hence I_D becomes larger, resulting in smaller drain lag [9].

CURRENT SLUMP

Next, we have calculated a case where V_G is changed from an off point. In this case, V_G is changed from the threshold voltage V_{th} to 0 V, and V_D is lowered from 10 V to V_{Don} (on-state drain voltage). V_{th} is defined as the gate voltage where the drain current I_D becomes 5x10^{-3} A/cm. Under these conditions, the device characteristics (not shown here) become similar to those shown in Fig.2, although some transients arise when only V_G is changed (gate lag). From these turn-on characteristics, we obtain a quasi-pulsed I-V curve.

In Fig.3, we plot the drain current (x symbols) at t = 10^{-8} sec after V_G is switched on, with V_{Don} (V_D) as a parameter. Fig.3(a) is for the case without a field plate, and Fig.3(b) is for the field-plate structure (L_{FP} = 1 μm, d = 0.1 μm). These curves are regarded as quasi-pulsed I-V curves with pulse width of 10^{-8} sec. Without a field plate, the pulsed I-V curve lies significantly lower than the steady-state I-V curve (solid line), indicating current slump and gate lag behavior. In Fig.3, we also plot another pulsed I-V curve (Δ symbols), which is derived from the data shown in Fig.2 (when only V_D is changed), indicating a large drain lag without a field plate. However, from Fig.3(b), we can see that by introducing a field plate, the current slump, drain lag and

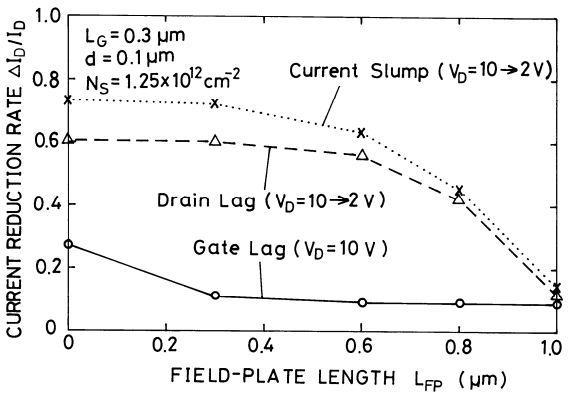

Fig.4 Current reduction rate $\Delta I_D/I_D$ due to current slump, drain lag or gate lag for GaAs MESFETs, with field plate length L_{FP} as a parameter. d = 0.1 μm. N_S = 1.25x10^{12} cm^{-2}.

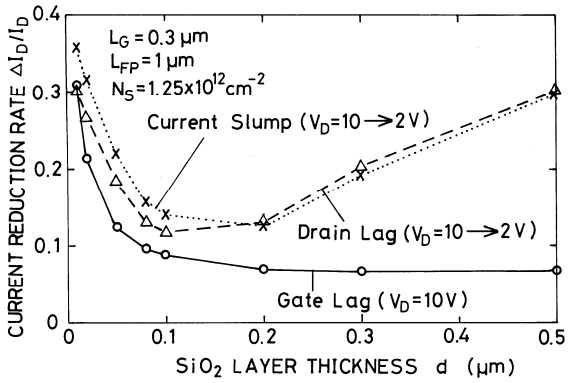

Fig.5 Current reduction rate $\Delta I_D/I_D$ due to current slump, drain lag or gate lag for GaAs MESFETs, with SiO_2 layer thickness d as a parameter. L_{FP} = 1 μm. N_S = 1.25x10^{12} cm^{-2}.

gate lag are all greatly reduced. In this case, the reduction of drain lag contributes to reducing the current slump.

FIELD-PLATE PARAMETER DEPENDENCE

The study also explored the dependence of lag phenomena and current slump on the field-plate length L_{FP} and SiO_2 layer thickness d.

Fig.4 shows the drain current reduction rate $\Delta I_D/I_D$ (ΔI_D: current reduction, I_D: steady-state current) due to current slump, drain lag or gate lag, as a function of field-plate length L_{FP}. Here, the thickness of the SiO_2 was held constant at d = 0.1 μm. The values of current slump and drain lag were simulated for the case where V_D is lowered from 10 V to 2 V. It is seen that when the field-plate length (L_{FP}) becomes longer (≥ 0.8 μm), the drain lag and current slump are reduced. This is because for longer field plate, the energy barrier between field-plate edge and drain, which is formed when V_D is lowered, becomes smaller. In the case when V_D is lowered from 10 V to 4 V, the reduction in drain lag and current slump starts at shorter lengths (L_{FP}).

Fig.5 shows the drain-current reduction rate $\Delta I_D/I_D$ due to current slump, drain lag or gate lag, as a function of SiO_2 passivation layer thickness d. Here, the field-plate length is held constant at L_{FP} = 1 μm. It is seen that when the passivation layer is thick, the existence of the field-plate has little effect, and the current slump and drain lag remain relatively large. For moderate passivation layer thicknesses, the current slump and drain lag are reduced greatly. This is because the surface state-related effects are reduced as described before. However, for thin d, the current slump and drain lag increase steeply. This may be due to the field plate beginning to act like a gate electrode. From this figure, it can be seen that there is an optimum thickness of SiO_2 passivation layer to minimize the surface-state-related current slump and drain lag in GaAs FETs.

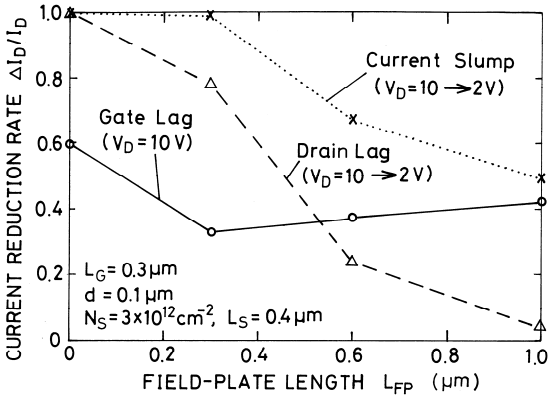

Fig.6 Current reduction rate $\Delta I_D/I_D$ due to current slump, drain lag or gate lag for GaAs MESFETs, with field plate length L_{FP} as a parameter. d = 0.1 μm. N_S = 3x10^{12} cm^{-2} and the surface-state length is 0.4 μm.

REMOVAL OF LAGS AND CURRENT SLUMP

Next, we modeled a case where a relatively large density of surface states (3x10^{12} cm^{-2}) exists only at the drain edge of the gate region. This situation can occur after the device has been stressed or due to device degradation.

Fig.6 shows current reduction rates $\Delta I_D/I_D$ due to current slump, drain lag, or gate lag, as a function of variable field-plate lengths L_{FP} where the passivation SiO_2 thickness is held constant at d = 0.1 μm. Here the length of surface-state region is set to 0.4 μm from the gate edge toward the drain. It is seen that when L_{FP} becomes longer than the length of surface-state region, the drain lag and current slump begin to decrease. The gate lag, however, is relatively insensitive to field-plate length.

Fig.7 shows calculated turn-on characteristics for a device with a longer field plate (L_{FP} = 1 μm) and a very thin passivation thickness (d = 0.01 μm). Here, V_D is lowered from 10 V to V_{Don} and V_G is changed from V_{th} to 0 V. Surprisingly, the slow current transients disappear, indicating that the lags and current slump are completely removed in this case. Fig.8 shows current reduction rates $\Delta I_D/I_D$ due to current slump, drain lag, or gate lag, as a function of passivation layer thickness d. As d becomes thin,

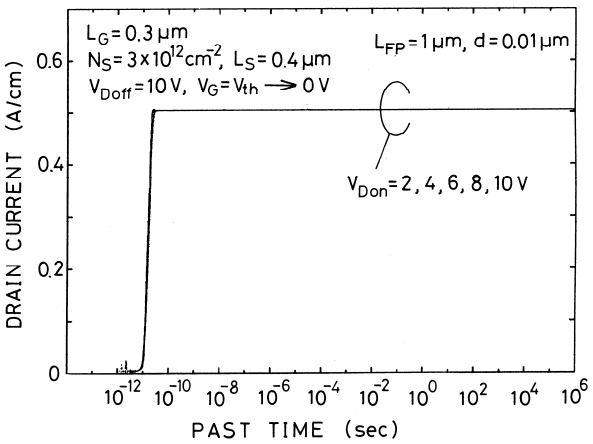

Fig.7 Calculated turn-on characteristics for L_{FP} = 1 μm and d = 0.01 μm when V_D is lowered abruptly from 10 V to V_{Don} and V_G is changed from V_{th} to 0 V. N_S = 3x10^{12} cm^{-2} and the surface-state length is 0.4 μm.

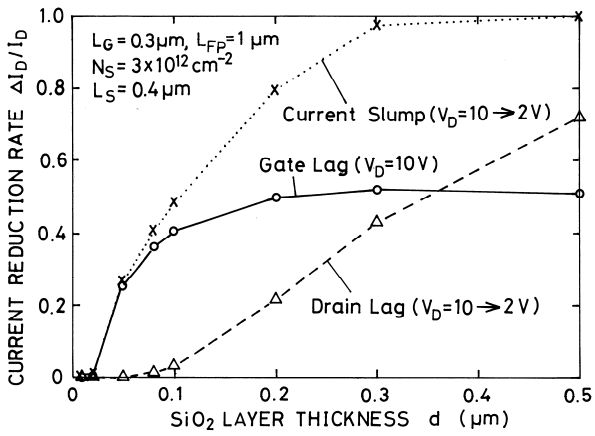

Fig.8 Current reduction rate $\Delta I_D/I_D$ due to current slump, drain lag or gate lag for GaAs MESFETs, with SiO_2 layer thickness d as a parameter. L_{FP} = 1 μm. N_S = 3x10^{12} cm^{-2} and the surface-state length is 0.4 μm.

the lags and current slump are reduced, and they are completely removed when d becomes thinner than 0.02 μm. This may be due to the field plate completely masking the surface-state effects. Practically, when d is thin, the gate parasitic capacitance will likely limit device performance, but this removal of current slump is still a very interesting result.

CONCLUSIONS

Two-dimensional transient simulations of the field-plate GaAs MESFETs have been performed in which surface states are considered. Quasi-pulsed *I-V* curves have been derived from the transient characteristics.

First, we have studied the case where relatively low surface state densities are considered on the entire region between source and gate and between gate and drain. It has been shown that the drain lag, gate lag and current slump due to surface states are reduced by introducing a field plate. The current slump has been shown to become smaller for longer field plates and for moderate SiO_2 layer thicknesses.

Next, we have studied the case where relatively large densities of surface states exist only at the drain edge of the gate region. It has been shown that the lags and current slump can be completely removed when the field-plate length becomes longer than the surface-state length and the SiO_2 passivation layer is very thin.

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ACRONYMS

L_G: gate length
L_{FP}: field-plate length
d: SiO_2 passivation layer thickness
N_{SD}: surface deep-donor density
N_{DA}: surface deep-acceptor density
V_D: drain voltage
V_G: gate voltage
V_{Dfin}: final drain voltage when V_D is lowered
V_{th}: threshold voltage
V_{Don}: on-state drain voltage
ΔI_D: drain-current reduction due to lag or current slump
I_D: steady-state drain current