High Mobility (210 cm^2/Vs), High Capacitance (7.2 $\mu F/cm^2$) ZrO_2 on GaN Metal Oxide Semiconductor Capacitor via ALD

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Keywords: Density of Interface Traps, Electron Mobility, high-k, dielectric constant, Atomic Layer Deposition (ALD)

Abstract

ZrO_2 has been deposited on GaN by atomic layer deposition. Chromium was sputtered and patterned on the ZrO_2 to create Metal Oxide Semiconductor Capactors (MOSCAPs). Capacitance voltage measurements yielded capacitance density of 7.2μF/cm^2, and a mobility of 210 cm^2/Vs. This is a fundamental step in the creation of a viable enhancement mode MOSFET.

Introduction

Gallium Nitride (GaN) is an III-V semiconductor material currently investigated for high frequency, high power electronics. GaN gives electrical engineers a wide variety of promising material properties including a high saturation velocity (v_s = 3x10^{17} cm/s), high critical electric field (Ec = 4.2 MV/cm) [1], and a large band gap (Eg = 3.4 eV).

Creating high quality dielectric-semiconductor interfaces is a critical step to achieve higher performance for GaN MOSFETs. Many different dielectrics have been investigated for their effects on interface quality. MOSCAPs can be used to investigate the effects of different dielectrics on electrical characteristics.

A number of different high-κ dielectrics have been recently investigated including HfO_2 [3], Sc_2O_3[4], Gd_2O_3[5], and La_2O_3 [6]. Many problems exist when using high-κ dielectrics. One such problem is the high parasitic conductance between the dielectric and gate, which can be reduced by using high-κ dielectrics with a high permittivity and a large band gap [6]. Recent investigation of MOCVD HfO_2 and ZrO_2 on GaN has shown low leakage current, and good capacitance characteristics [7].

When evaluating the different problems with high-κ dielectrics, ZrO_2 stands out as a promising gate dielectric. With use of improved deposition techniques, it becomes possible to deposit very low defect density oxides with good interface characteristics via Atomic Layer Deposition (ALD). In the following, we present ZrO_2 deposited via ALD on GaN.

MOSCAP structure and Fabrication

The GaN/Sapphire templates were acquired from Kyma Technologies. The templates consisted of 5 μm thick GaN grown on a proprietary buffer layer and a 2 inch sapphire substrate.

Two different samples were prepared with the ZrO_2 gate dielectric deposited onto the GaN layer via O_2 plasma assisted ALD for 40 and 68 cycles at 100 ^{o}C and 1 Torr. The thickness was measured *in situ* and post deposition using an ellipsometer on a silicon wafer for calibration and predicted to be 6.9 nm and 10 nm respectively. Transmission Electron Microscopy (TEM) of the GaN template was done to independently determine the thickness of the thicker sample, and found sample was actually closer to 9.2 nm. Further work must be done to determine the growth rate, and quantify the offset. Following the ALD approximately 100 nm of Cr was deposited by sputtering. It was then annealed at ~ 400 ^{o}C for 15 minutes. The contacts were patterned by contact lithography using HPR 504 positive photoresist. Figure 1 illustrates the top view and cross sectional layout of the MOSCAP.

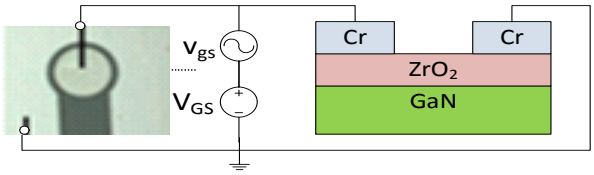

Figure 1: The top view of a typical 100 x 1000 um MOSCAP taken with a confocal microscope, an illustrated cross section with test set up for typical measurements..

Results and Discussion

The electrical characteristics were measured using the Keithley 4200-SCS. As is well known when testing hetero-epitaxial wide band-gap semiconductors, the use of backside contacts is

prohibitive but what was unknown at the time of experimental design was the quality of the gate oxide would allow leakage less than 1 A/cm^2 for the thinner structure. Because buffered layers stored a significant charge, an electrical short was induced between the source and the substrate with a significant voltage pulse (5 V) over a short period of time (1μs). This effectively created a path for electrons to supply the accumulation layer with minimal interference with the measurement.

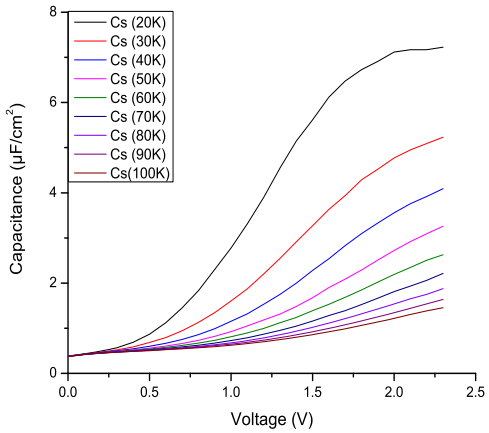

Figure 2: Spreading effects lower the effective capacitance as the measurement frequency increased. Lower frequencies produce the best reflection of the actual capacitance of the dielectric film.

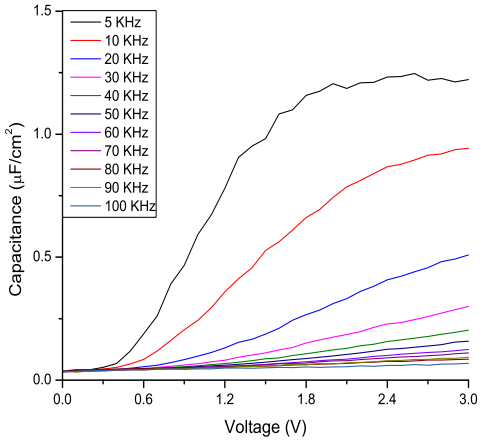

Figure 3: The capacitance density was 1.2μF/cm^2 at 5 KHz. Spreading effects were also observed on the thicker sample.

The capacitance density in the thinner sample was 7.2μF/cm^2 (20 KHz), while the thicker sample was 1.2μF/cm^2 (5 KHz) as seen in Figure 2 and Figure 3. Spreading effects lowered the effective capacitance as the frequency increased. Analysis of this effect verified a distributed model [8]. The net effect is that the lowest frequency produces the most reliable capacitance measurement. The added benefit of this variance w.r.t frequency is that it can be used to determine the mobility of the carriers in the accumulation layer.

Using the thickness determined through the TEM and equation 1, it was possible to estimate the dielectric constant, ε_r, of the thicker sample. The accumulation layer thickness was estimated 0.75 nm from models that use different effective masses for the dielectric [9] and estimate the thickness due to the quantum repulsion resulting of the dielectric. The value used in calculation is an estimate and the accumulation layer thickness observed in the simulations from 0.5nm to 1.0nm.

$$C_{Measured} = \varepsilon_o \left(\left(\frac{\varepsilon_r (ZrO_2)}{t_{oxide}}\right)^{-1} + \left(\frac{\varepsilon_r (GaN)}{t_{accumulation}}\right)^{-1} \right)^{-1} \quad (1)$$

The estimated dielectric constant, ε_r, was 14. This agrees with work previously done [10] [11]. The dielectric constant for the thinner sample was not determined as of this point. Using the estimated thickness from the ALD growth rate on Silicon produced ε_r in excess of 70, which is not easily explainable with normal means. A TEM will be done in future work, to determine the effective thickness of the actual film. We anticipate a significant delay in growth initiation that produces a much thinner oxide than would be expected with the number of cycles used in the Atomic Layer Deposition.

Figure 4 shows a voltage sweep of the thinner sample at 20 KHz. Further investigation of the CV characteristics revealed a hysteresis of less then 6 mV, indicating low density of interface traps, D_{it}. The level of hysteresis increased with the oxide thickness. The thicker sample displayed a more pronounced hysteresis then observed in the thinner sample. As seen in Figure 5, the worst case was close to 50 mV while other MOSCAPs on the same sample displayed much lower hysteresis. Typically values were on the order of 30mV. If

this observed defect density were to vary with thickness (or capacitance) it would be indicative of charge imbedded in the oxide. In this case we do not see that kind of relationship.

$$D_{it} = \Delta V \frac{C_{ox}}{qE_g} \quad (2)$$

Using equation 2, the Dit was estimated using the hysteresis found in the CV curve [12]. We found a Dit = 3.20×10^{10} $eV^{-1}cm^{-2}$ at 20 KHz on the thin sample. The thicker sample produced a Dit = 5.0×10^{10} $eV^{-1}cm^{-2}$(typical, as high as 1.0×10^{11} $eV^{-1}cm^{-2}$). This is for all intents and purposes an equivalent value estimated for interface traps, regardless of thickness.

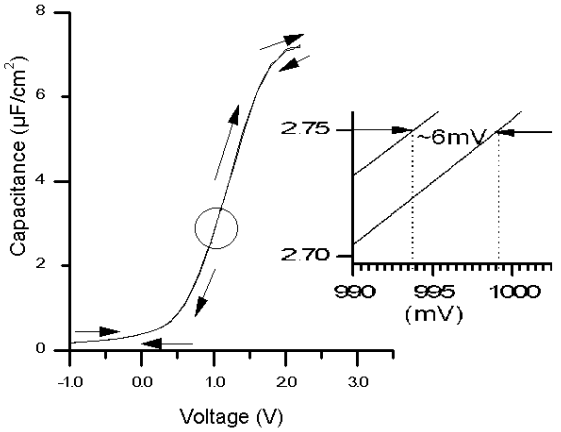

Figure 4: A CV sweep of the thinner at 20 KHz revealed the MOSCAP displayed little hysteresis.

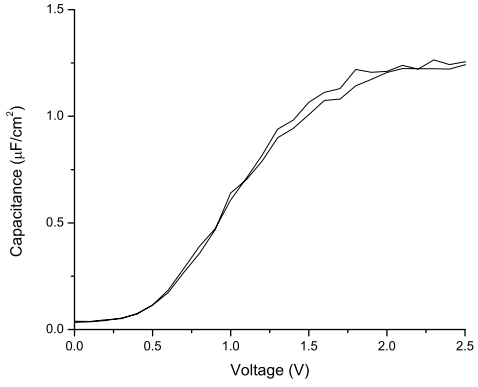

Figure 5: A CV sweep of the thicker MOSCAP at 5 KHz revealed a larger hysteresis then the thinner sample displayed.

Through analysis of the frequency dependent C-V characteristics, a mobility model was created for the GaN MOSCAP [13]. This revealed that the peak electron mobility reached 210 cm^2/Vs. This was consistent with both samples as seen in Figure 6. What this near ideal mobility also shows is that the interface is very much free of excess traps. The analytical model presented is an adaptation of the common universal mobility model used for silicon MOSFETs when considerations are taken for differences in bulk mobility and substrate dielectric constant. What should be pointed out is that the mobility vs. field characteristics was the same regardless of center electrode dimension, or thickness of dielectric which supports the measurement technique and method of reporting capacitance.

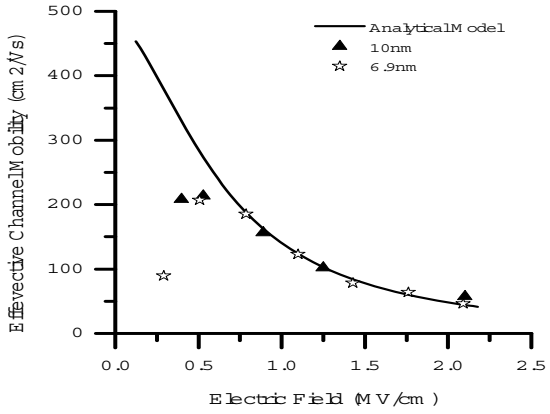

Figure 6: The effective electron mobility through the GaN is consistent for both the 6.9nm and 10 nm oxides.

IV measurements are shown in Figure 7 for the thicker and thinner sample. Temperature measurements performed on the thinner sample revealed minimal temperature dependence in the forward direction as seen in Figure 8. Similar temperature measurements performed on the thicker sample displayed a slightly higher level of temperature dependence. What is true in both cases is that the temperature dependences is what should be expected for an oxide that is limited by direct tunneling in forward bias (electrons travelling from substrate to gate) and is limited by recombination currents in reverse direction. The deposition technique and pre-treatment has the potential to produce as a semiconductor interface with extremely low levels of defects.

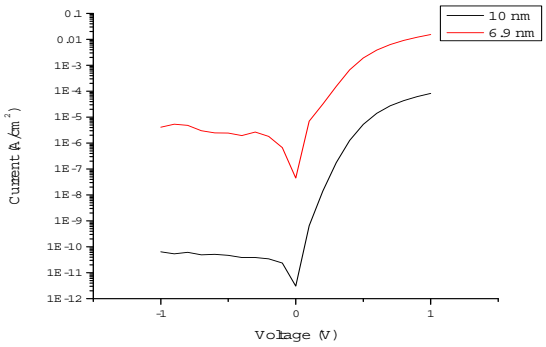

Figure 7: The gate oxides display near ideal tunneling current that scales appropriately with oxide thickness.

Conclusion

A low D_{it} ZrO_2 oxide was deposited onto GaN/Sapphire templates using ALD. The electrical characteristics measured displayed high capacitance densities (7.2 μF/cm^2) and mobility (210 cm^2/Vs) achieved for multiple thicknesses. IV measurements conducted on the samples revealed low gate oxide leakage, with minimal temperature dependence. The measurements indicate a ZrO_2 oxide with extremely low D_{it} and a good ZrO_2/GaN interface.

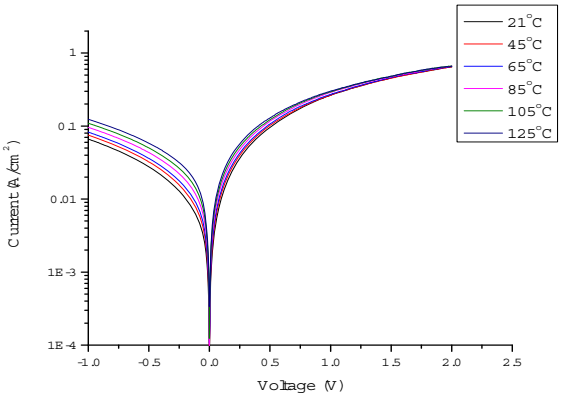

Figure 8: Variations in temperature had little effect on the thinner gate oxide consistent with direct tunneling.

Acknowledgements

The authors would like to thank National Science Engineering and Research Discovery Program, and the University of Alberta Electrical and Computer Engineering Department and Department of Material Science and Chemical Engineering. We would like to acknowledge Ben Bathgate for help with measurement set ups. We would also like to thank Alex Ma for help in preparation of the samples.

References

[1] Ozbek, A.M., et al., "Finite-Zone Argon Implant Edge Termination for High-Voltage GaN Schottky Rectifiers", IEEE ELECTRON DEVICE LETTERS, VOL. 32, NO. 10, Oct 2011

[2] B. J. Baliga, "Power Semiconductor Device Figure of Merit for High-Frequency Applications" IEEE Electron Device Letters 10 (1989) pg. 455

[3] Chang, Y., et al., "Structural and electrical characteristics of atomic layer deposited high kappa HfO_2 on GaN". Appl. Phys. Lett., 2007. 90(23)

[4] Cho, H., et al., "Influence of gate oxide thickness on Sc_2O_3/GaN MOSFETs". Solid-State Electronics, 2003. 47(10): p. 1757-1761.

[5] Johnson, J., et al., "Gd_2O_3/GaN metal-oxidesemiconductor field-effect transistor". Applied Physics Letters, 2000. 77(20): p. 3230-3232.

[6] J. S. Jur*., et al, "Epitaxial Rare Earth Oxide Growth on GaN for Enhancement-mode MOSFETs" CS MANTECH Conference, 2008

[7] Abermann, S., et al, "MOCVD of HfO_2 and ZrO_2 high-k gate dielectrics for InAlN/AlN/GaN MOS-HEMTs", Semicond. Sci. Technol. 22 (2007) 1272–1275

[8] von Hauff, P., et al, "High Capacitance Density (7.2μF/cm2) ZrO_2 on GaN Metal Oxide Semiconductor Capacitor with low Hysteresis via Atomic Layer Deposition", App. Phys. Lett., submitted Feb. 2012.

[9] Bothe, K., et al, "Underlying Design Advantages for GaN MOSFETs compared with GaN HFETs for Power Applications", Submitted Feb. 2012.

[10] Gu. X, Izyumskaya. N, Avrutin. V, Xiao. B, Morkoc, H., "Epalitaxial growth of ZrO_2 on GaN templates by oxide molecular beam epitaxy", App. Phys. Lett 2007. 90(2)

[11] Lubig. A, Buchal. CH, Guggi. D.," Epitaxial growth of monoclinic and cubic ZrO_2 on Si(100) without prior removal of the native SiO_2" Thin Solid Films 1992 vol 217(1-2)

[12] Witczak, S.C, et al, "An Experimental Comparison of Measurements Techniques to Extract Si-SiO2 Interface Trap Density", Solid State Electronics, 1992 35(3) 345-355

[13] K. Bothe et al, "Capacitance Modeling and Characterization of Planar MOSCAP devices for Wide Bandgap Semiconductors with High-K Dielectrics", IEEE Transactions on Electron Devices, submitted Feb. 2012

ACRONYMS

ALD – Atomic Layer Deposition

TEM – Transmission Electron Microscope

MOSCAP – Metal Oxide Semiconductor Capacitor

MOSFET – Metal Oxide Semiconductor Field Effect Transistor

GaN – Gallium Nitride

ZrO_2 – Zirconium Oxide

D_{it} – Density of Interface Traps