Threshold Voltage Control of Recessed-Gate III-N HFETs Using an Electrode-less Wet Etching Technique

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Abstract

We reported an electrode-less wet etching technique that achieves smooth etched surface and uniform recess depth for recessed-gate AlGaN/GaN HFETs. Constant etching rate and high etching selectivity between III-N layers were observed. After wet etching, the threshold voltage (V_{th}) of HFETs was shifted from -6V to 0.06V and the maximum transconductance was increased from 86 mS/mm to 116 mS/mm. The sub-threshold slope was reduced from 119 mV/decade to 83 mV/decade. The standard deviation of V_{th} is 177mV measured from 60 fabricated HFETs. Maximum drain current ($I_{D,max}$) of 420 mA/mm was achieved at V_{GS} = 4 V. The results suggest that electrode-less wet etching can achieve precise control of threshold voltage for E/D-mode III-N HFETs.

INTRODUCTION

GaN-based field-effect transistors have been a focused topic for its high-current-drive, high switching-frequency, and high breakdown voltage [1,2]. Most of the reported devices have normally-on (D-mode) characteristics with threshold voltage of -3 to -6 V [3-5]. In mixed-signal integrated circuits and monolithically integrated circuits, E/D mode GaN HEMT MMICs are interested research topics. To control the threshold voltage of GaN-based HFETs, several techniques, including fluorine-treated HFETs[6], p-type III-N gate[7,8], and tunnel junction HFETs[9], have been demonstrated.

The recessed-gate structure is considered advantageous over other approaches for its simplicity and the ability to achieve higher transconductance. Plasma-enhanced dry etching techniques were typically used for AlGaN/GaN and InAlN/GaN HFETs [10,11]. However, recess depth control and etching damage are challenging for dry-etching techniques. Photo-electrochemical wet etching techniques with electrodes [12] and without electrodes [13,14] were also studied on III-N materials. Nevertheless, these wet-etching techniques suffer from non-uniform etching that result in rough etched surface or threshold voltage uniformity issues if the process is not well controlled.

In this study, we report a new electrode-less wet etching technique using KOH-based solution. It shows the ability to achieve smooth etched surface and potentially uniform device threshold voltage control in III-N HFETs. Constant etching rate and high etching selectivity between different III-N layers were also observed. Uniform recess depth and smooth etched surface were achieved. The fabricated HFETs show that the threshold voltage can be shifted from -6V to 0.06V after wet etching. The transconductance is also increased from 86 mS/mm to 116 mS/mm before and after the recessed-gate etching, respectively. Accodringly, the sub-threshold slope is reduced from 119 mV/decade to 83 mV/decade. The statistical data show that the average and standard deviation of V_{th} is -0.1V and 177 mV, respectively, from 60 fabricated recessed-gate HFETs. High current drive (420 mA/mm), high breakdown voltage (> 1.2 kV) and low specific on-resistance (6.6 mΩ-cm^2) were measured on fabricated 0.3-mm-wide recessed-gate HFETs. The 10mm-wide device shows $I_{D,max}$ of 3.7 A at V_{GS} = 4V with specific on-resistance of 4 mΩ-cm^2. Compared to other approaches, these results indicate that the electrode-less wet etching could be a viable approach to achieve desire threshold voltage with good device performance for III-N HFETs.

LAYER STRUCTURE AND DEVICE FABRICATION

The AlGaN/GaN HFET wafer in this study was grown by a commercial epi-vendor. The layer structure consists of un-doped AlGaN, a thin AlN layer and a GaN buffer layer on a 3-inch Si substrate. The fabrication processing of AlGaN/GaN HFETs started from the mesa isolation. After the mesa isolation, a PECVD SiO_2 layer was deposited to serve as the electrode-less wet etching mask. A mixture of potassium persulfate and potassium hydroxide was prepared. The ultraviolet light was used to catalyze the electrolyte without the need for additional current source during the etching [15]. After the recessed-gate etching, TiAl-based ohmic metal was deposited and annealed for the drain and source contact pads. Nickel gate electrodes were deposited using an electron-gun evaporator. The transistors were then passivated by

Benzocyclobutene (BCB), followed by the via-hole opening. Finally, thick Metal-1 layer was deposited for interconnects. The devices in this set of study have a range of gate width (W_G) from 0.3 mm to 10 mm.

RESULTS AND DISCUSSION

Shown in Figure 1 is a plot of the recess depth as a function of the recessed-gate etching time measured by atomic force microscopy (AFM). At the beginning of wet etching, a constant etching rate of 1.1 nm/min was measured until the recess depth reached ~30 nm. After 30 minutes of etching, the recess depth remained unchanged. The result indicates that high etching selectivity can be achieved between AlGaN and AlN layers in this wet-etching system to achieve high uniformity across the wafer.

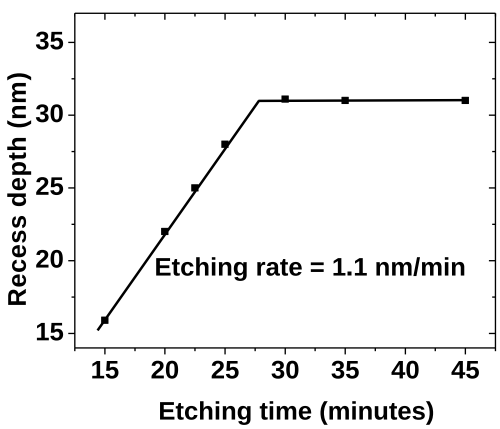

Figure 1 The recess depth versus etching time of the recessed-gate process on AlGaN/GaN HFETs.

The surface morphology of the etched and as-grown area was measured by AFM, as shown in Figure 2. The etched area has an RMS surface roughness of 0.37 nm in a 1×1 μm^2 2-dimensional areal scan, which is comparable to that of 0.255 nm on the as-grown surface. It shows that a smooth etched surface can be achieved with this unique wet etching approach.

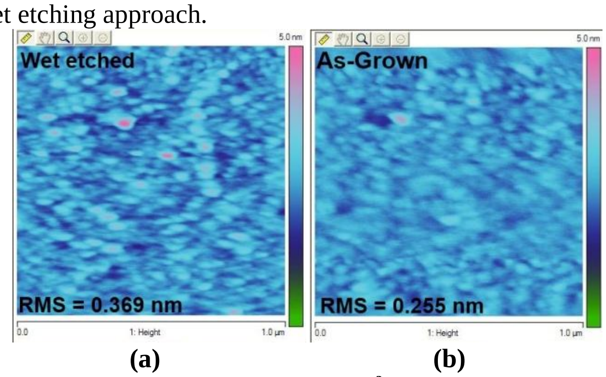

Figure 2 The surface morphology in 1×1 μm^2 area measured by AFM on (a) the etched surface and (b) the as-grown surface

For comparison, AlGaN/GaN HFETs with and without the recessed-gate etching were fabricated. The measured I_D-V_{GS} curves of a 0.3-mm-wide HFET (L_{GD} = 13 μm and L_G = 3 μm) with and without recessed-gate etching at V_{DS} = 10 V are shown in Figure 3. The threshold voltage (V_{th}) is determined at I_{DS} = 1 mA/mm. For as-grown HFETs, V_{th} = -6 V were measured while V_{th} is shifted to 0.06 V after the recessed-gate etching. The on-off ratio is approximately identical (2×10^6) on both devices while the maximum transconductance ($g_{m,max}$) is increased from 86 mS/mm to 116 mS/mm on the recessed-gate HFET due to reduced barrier thickness. The off-state drain leakage current remains < 200 nA/mm for devices with and without the recessed-gate etching. These results confirm that good Schottky gate properties were achieved on recessed-gate devices.

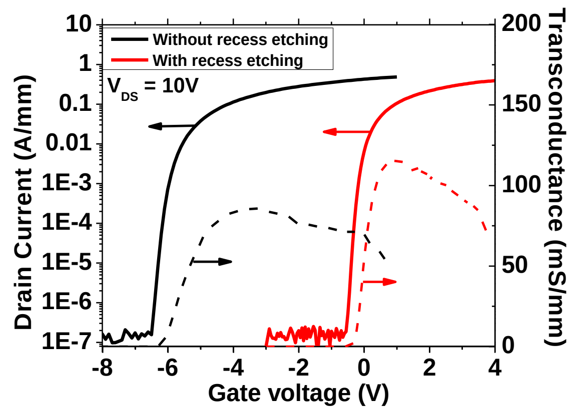

Figure 3 The measured I_D-V_{GS} curves of 0.3-mm-wide HFETs with and without recessed-gate etching.

For the recessed-gate devices, the sub-threshold slope (S) is reduced from 119 mV/decade to 83 mV/decade. The sub-threshold slope of can be expressed as:

$$S \cong \frac{kT}{q} \ln(10)\left(1 + \frac{C_Q + C_{it}}{C_i}\right)$$

where C_i is the AlGaN capacitance, C_Q is the quantum capacitance, and C_{it} is the interface-trap capacitance[16]. At deep sub-threshold region where we calculate the sub-threshold slope, C_Q is much smaller than C_i due to the Fermi–Dirac distribution so it is negligible [11]. Assuming the recessed-gate etching stops at the AlN layer, the interface-trap capacitance after the wet etching is 3 μF/cm^2 while that on the as-grown HFETs is 0.2 μF/cm^2. The higher interface-trap capacitance suggests that some surface damage may still exist in the recess region. However, this capacitance may be over-estimated. More detailed studies will be required to reveal the impact of wet etching on the surface properties.

To investigate the threshold voltage uniformity, 60 devices with different W_G's (3,5,6, and 10 mm) were measured. Figure 4 shows a histogram of V_{th} for the fabricated HFETs. The data points were collected from on a wafer piece with an area of 1 × 0.5 cm^2. The averaged V_{th} is -0.1 V and the standard deviation for V_{th} is 177 mV. The relatively tight control of V_{th} suggests that uniform recess depth can be achieved with the electrode-less wet etching.

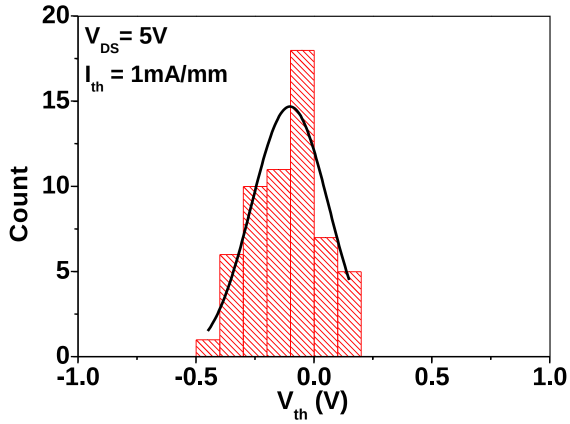

Figure 4 The histogram of measured threshold voltages of HFETs

In Figure 5, the measured I_D-V_{DS} family curves for as-grown and recessed-gate HFETs with W_G = 0.3 mm and L_{GD} = 13 μm are also shown for comparison. Compared to the as-grown HFETs with $I_{D,max}$ > 510 mA/mm at V_{GS} = 1V, recessed-gate HFETs showed lower $I_{D,max}$ of 420 mA/mm at V_{GS} = 4 V. The specific on-resistance ($R_{on}\cdot A$) of 6.6 mΩ-cm^2 for the recessed-gate HFET is higher than that for the as-grown D-mode HFETs (4.7 mΩ-cm^2). Higher $R_{on}\cdot A$ and lower $I_{D,max}$ may be attributed to the higher access resistance in the recessed gate region.

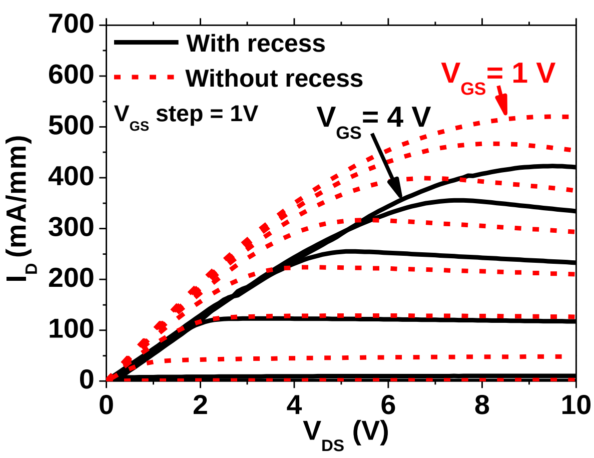

Figure 5 The measured I_D-V_{DS} curves of 0.3-mm-wide HFETs with and without the recessed-gate etching.

The recessed-gate HFETs were also measured in an Agilent B1505A digital curve tracer with a pulse width of 100 μs and a duty cycle of 2%. Shown in Figure 6 are the family curves of an AlGaN/GaN HFET with W_G = 10 mm. A maximum current of 3.7 A, corresponding to 370 mA/mm current density, is achieved at V_{GS} = 4 V. The lower current density, when compared to 0.3-mm-wide devices, may be attributed to current spreading issue in multi-finger devices. Nevertheless, $R_{on}\cdot A$ = 4 mΩ-cm^2 was measured at V_{DS} = 1 V and V_{GS} = 4 V.

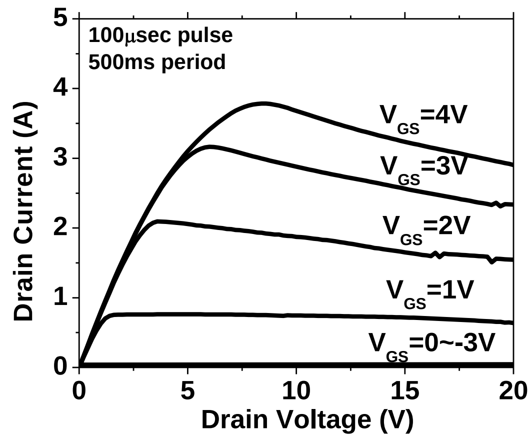

Figure 6 On-state characteristics of a fabricated device with W_G = 10mm and L_{GD} = 13μm.

Figure 7 shows a competitive device performance comparison for E-mode GaN-based field-effect transistors using different gate engineering approaches. Using the electrode-less wet etching recessed-gate technique, a 0.3-mm-wide HFET with L_{GD} = 13 μm showed breakdown voltage of 1200V and $R_{on}\cdot A$ of 6.6 mΩ-cm^2. It corresponds to a figure of merit (BV^2/R_{on}) of 240 MW/cm^2.

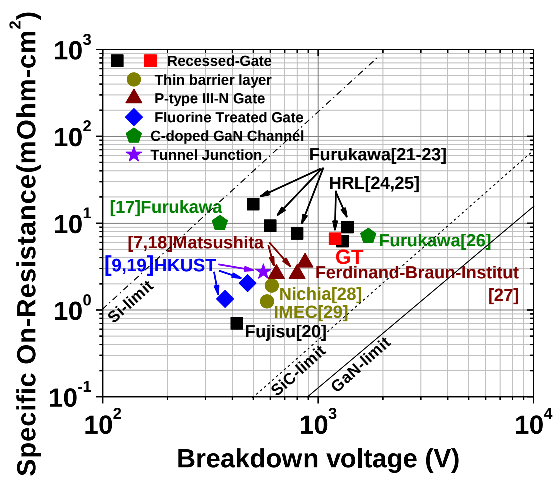

Figure 7 Specific on-resistance versus breakdown voltage for E-mode III-N high power transistors with different threshold voltage control approaches[7,9,17-29].

CONCLUSIONS

In summary, we report a potentially manufacturable electrode-less wet etching technique to fabricate recessed-gate AlGaN/GaN HFETs. Smooth etched surface and uniform threshold voltage can be achieved in these devices.

High current drive and low specific on-resistance were achieved on the fabricated recessed-gate HFETs. High breakdown voltage (> 1.2 kV) was also measured on the 0.3-mm-wide HFETs. The results suggest the novel electrode-less wet etching approach can be used in III-N HFETs for E/D-mode device implementation.

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ACRONYMS

HFET: Heterojunction Field Effect Transistor
D-mode : Depletion mode
E-mode : Enhancement mode
W_G: Gate width
L_{GD}: Gate-to-drain distance
BV: Drain-to-source breakdown voltage
$R_{on} \cdot A$: Specific on-resistance