Evaluation of through wafer via holes in SiC substrates for GaN HEMT technology

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ABSTRACT

GaN technologies arrive at production of IC manufacturers with quite fast evolving processes. Especially backside processes are challenging due to the used substrate materials. There exists a lot of experience and know-how in backside processing of GaAs and Si substrates and there is know-how of SiC processing. But there is not very much experience in the integration of a via hole process in thinned SiC substrates with a active GaN EPI layer in a manufacturing area. This work will present an evaluation of a SiC via hole process for GaN HEMT technology in terms of quality, integration, reliability and packaging process.

The via hole etching process is applying an aluminium hard mask either structured by lift off or by dry chemical etch. These two process variants differ in via hole quality and reliability. The impact of the via hole shape on the internal stress of the metal interconnection layer will be investigated. Also the etch rates and selectivities to the surrounding materials of the SiC ICP etching process evaluation will be shown.

Residues in the via holes are evaluated and wet chemical treatments to remove the via side wall residuals will be described. The residues have been analysed by XPS explaining their generation during via hole etch. Reliability tests and packacking tests of the different process variants have been done revealing the impact of the residues and via hole patterns.

INTRODUCTION

The ion energy of the plasma process has to be very high in order to crack the Si – C bonds. That means the process has to be mainly physically assisted by high dissipation of temperature in order to build volatile etch products. The SiC dry chemical etch takes place in a state of the art ICP plasma tool using SF6/O2 . All these aspects lead to a mask that has to withstand high temperature, physical ion energy and oxygen content of the plasma.

As fluorine chemistry is used for the SiC etch there is no way to use dielectrics like silicon oxides or nitrides due to their low selectivity. That means a metal or a metal compound hard mask has to be used.

In this work an aluminum hard mask is used to produce high quality through wafer via holes in SiC substrates. The high ion energy leads to high temperature dissipation during the via hole process which leads to redeposition processes of the aluminum and build up of Al with chemical bonds to fluorine. These side wall residues have to be removed by wet chemical treatment to avoid later delamination of the metal inside the via hole. Adequate roughness of the via side wall reduces the risk of cracks in and voids in between the metallisation and the SiC.

Finally the reliability in terms of metal delamination can be improved by choosing a circular instead of a rectangular via hole pattern.

PROCESS FLOW

The hard mask process has a strong impact on the via hole quality. Two variants of Al hard mask definitions by 1)dry chemical etch and 2) a lift off process are described in figure 1.

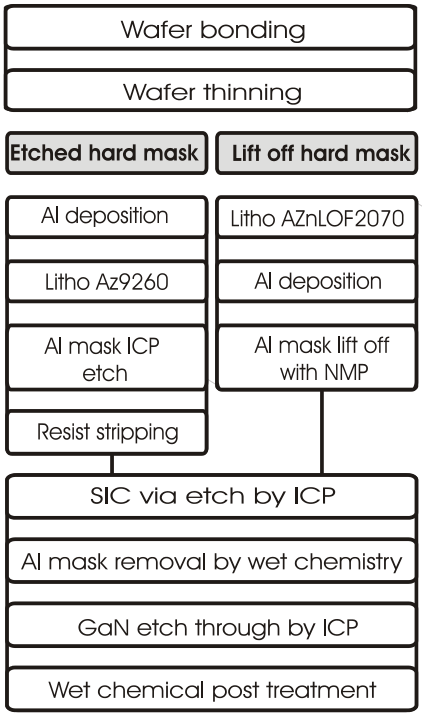

fig.1: process flow Via hole process module with etched and lift off hard mask

The following paragraphs describe the improvement of the processes for the Al hard mask and the wet chemical removal of the hard mask after the dry chemical SiC etching. The optimisation focusses on voids and metal delamination inside the via holes.

IMPACT OF SOFT AND HARD MASK ON VIA HOLE SIDE WALL

The quality of the via hole profile is different for a dry etched or lifted hard mask as described before. Figure 2 shows the cross section view of an ICP etched hole applying a lift off aluminum mask on the one hand and a dry etched mask on the other. The roughness of the mask edge in case of the lift off process lead to spikes and voids behind the metal in the via hole.

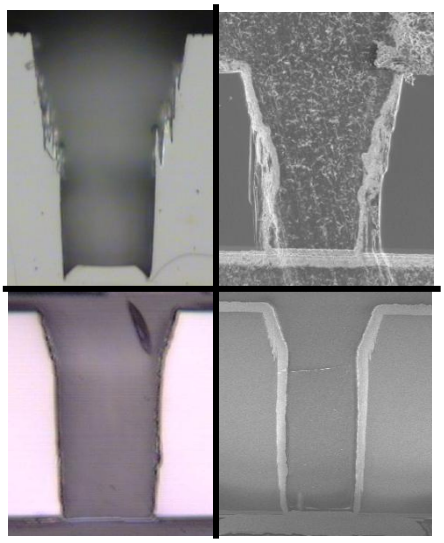

fig.2: Via etched by ICP plasma process – Al mask by lift off (top) and etched mask (bottom)

Due to the high selectivity of SiC:Al being around 22:1 during the silicon carbide dry etch step even a low mask edge roughness leads to big spikes at the via side wall. Therefore the profile of the Al edge has to be perpendicular and if possible without any mask edge foot. The hard mask thickness is 8 µm before and around 3 µm after the SiC etch. The SiC etch rate is 0.6 µm/min, with an etch time of 180 min and an overetch of 10% is applied.

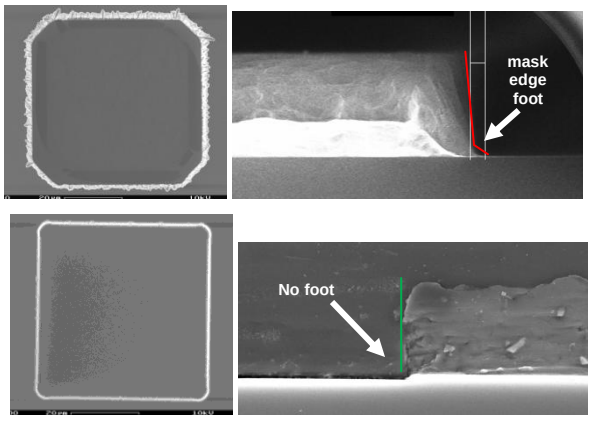

fig. 3: Al mask opening (left) and profile (right) for lifted (top) and etched (bottom) hard mask

In order to reach a perpendicular mask edge by plasma etching, the resist opening has to show a very steep profile. The stabilisation of the resist slope

is built by the first step of the Al mask ICP etch through the polymerisation of a thin layer of the resist. By applying this plasma the resist can withstand the temperature during the Al mask etching, consequently leading to a steep slope in the aluminium openings. A post bake after development for resist stabilisation is not possible as the slope of the resist tends to reflow. The process change towards the etched hard mask lead to void free metallisation inside the via hole.

METAL ADHESION INSIDE THE VIA HOLE

The mechanical integrity of the back side metallisation plays a major role for the assembly of the chip, in th case it is being soldered. The MMIC has to withstand a temperature budget of around 280°C - 340°C for several minutes at a soldering reflow process. During the development it was observed that at temperature storage and assembly tests metal peels off inside the via hole.

X-ray analysis of soldered dies as in figure 4 show delamination of the metal and around the affected via hole the build up of a void in the solder.

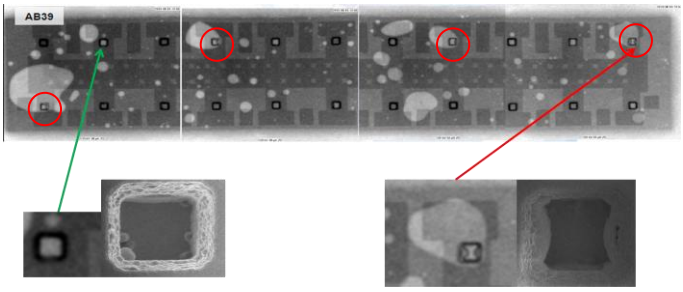

fig. 4: x-ray analysis of soldered die show delamination effects of metal inside the via (right) and non affected (left)

Further analysis and tests show that side wall residues redeposited during the SiC dry etch may cause the metal delamination (figure 5).

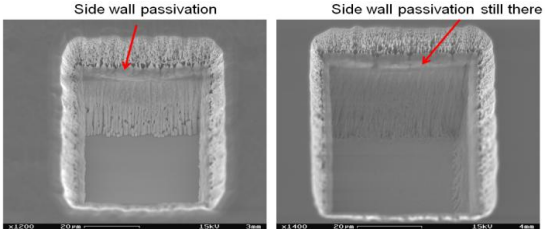

fig. 5: SEM top view of via hole after SiC etch (left) and after GaN etching (right) variant B

The XPS analysis on the via side wall shows residues with a chemical compound of Al fluorites. The analysis of the atomic concentration of the side wall passivation results in high amounts of fluorine and aluminum after the SiC and GaN dry etch compared to that of the fracture plane of the SiC substrate (figure 6).

These residues were built by the Al mask and fluorine gas during etching and redeposited on the side wall. The following wet chemical removal of the Al mask and the chlorine plasma for the GaN etch does not effectively remove the side wall passivation. The applied wet chemical post SiC via treatment (called variant B) has to be optimized regarding the chemical solubility of Al_xF_y compounds.

	reference	via side wall
C1s	51.1	7.6
O1s	9.2	7.2
F1s	-	**60.6**
Na1s	-	4.3
Al2p	0.2	**17.5**
Si2p	39.5	2.9

fig. 6: atomic concentration [%] of elements on the via side wall analysed by XPS

The process variant A of the wet chemical removal of the Al hard mask was developed in order to remove the residues. Furthermore the mechanical stress inside the metallisation is assumed to be higher for rectangular vias than for circular ones. Both changes were compared to each other in order to understand the mechanism of the failure mode (figure 7).

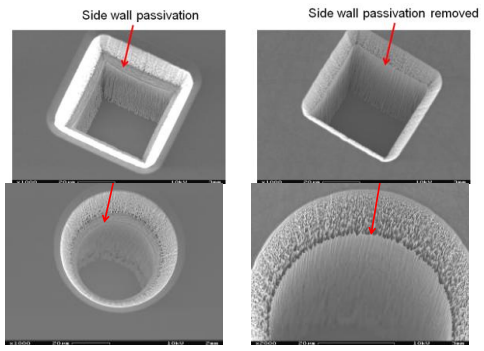

Fig. 7: SEM top view of via hole after SiC etch (left) and after GaN etching (right) with rectangular (top) and circular vias (bottom) variant A

The temperature storage at 300°C of wafers processed by variant B (former process) revealed the same failure mode defect by the interim via contact resistance measurement and following SEM inspection. As shown in figure 8 the wet chemical treatment of variant A shows no increase of the resistance and no metal delamination.

Increasing resistance can be explained by metal cracks at the contact area to the front side pad. The metal peel off happens locally with defect generation inside the via holes applying variant B process on circular vias. This test shows that circular vias with residues behind the metal withstand metal delamination from the whole side wall but the residues lead to local delamination of the metal and lead to cracks after temperature storage in case of circular patterned vias. This means that circular via holes show lower mechanical stress in the interface layer metal and side wall.

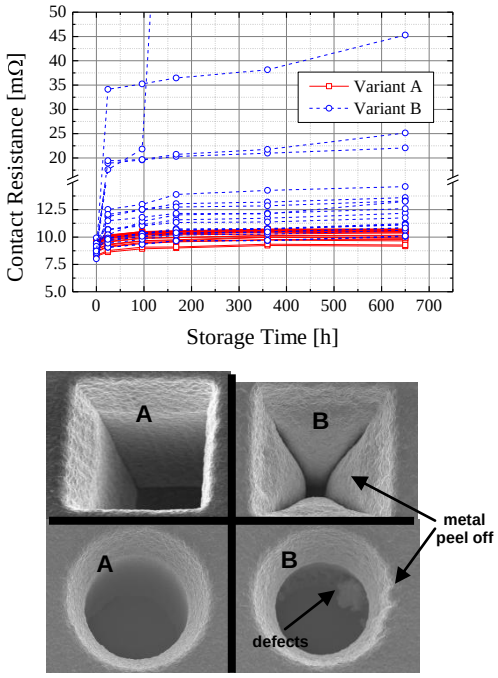

fig. 8: Contact resistance measurement vs storage time (top) and SEM inspection after storage (bottom) of processed vias variant A and B

Additional X-ray analysis show a low solder void rate and no metal delamination after the process changes as shown in figure 9.

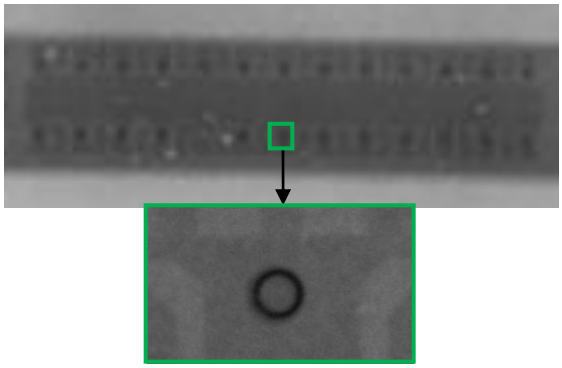

Fig 9: X-ray of new via post treatment process A and circular vias

Not removing the residues in the via holes show a significant impact on the interconnect reliability as shown in the temperature storage data and the x-ray analysis after the soldering process. Using circular patterned vias instead of rectangular additionally reduced the risk of reliability problems for the through wafer via interconnect.

CONCLUSION

This work shows a process approach to produce high quality and reliable via holes in SiC for GaN HEMT MMICs. Applying an aluminum hard mask for SiC via hole etching with a focus on the mask creation process and wet chemical via treatment. Various methods have been applied in order to reveal the impact of the via hole process module and its integration.

ACKNOWLEDGEMENTS

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