2 kV Breakdown Voltage GaN–on-Si DHFETs with Sub-micron Thin AlGaN Buffer

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Abstract

We present a cost effective approach to realize high breakdown voltage (V_{BD}) of AlGaN/GaN/AlGaN double-heterostructure FETs (DHFETs) having sub-micron thin AlGaN buffer layers on Si (111) substrates by Si removal. We observe that after Si removal, the V_{BD} of buffers and devices are enhanced and independent for different buffer thicknesses (600 nm, 1 µm and 2 µm). The buffers and devices V_{BD} show electric field strength of ~2.5 MV/cm and ~1 MV/cm respectively for all the buffer thicknesses. A device with L_{GD} = 20 µm having a buffer of only 600 nm thick, shows a V_{BD} of over ~ 2000 V after Si removal. Without Si removal, however, very thick buffer layers are needed to achieve such a high V_{BD}.

Introduction

GaN-HEMTs are foreseen to contribute significantly towards improved efficiency and downsizing the dimensions of power supplies since the devices have the potential of realizing high breakdown voltages (V_{BD}), low on-state resistances (R_{ON}) and high switching frequencies. AlGaN/GaN/AlGaN DHFETs device architectures are very promising for high power applications because of the improved carrier confinement and higher V_{BD} of the AlGaN buffer [1-2]. Si is the primary choice for III-N epitaxial growth because of its low cost and large size availability [3-4]. However, devices fabricated on Si substrates show a saturation of the breakdown voltage due to conduction from source-to-drain across the AlN/Si interface [5-8]. A technique to enhance the V_{BD} is to increase the III-N buffer thickness [9-10]. To obtain a V_{BD} of over 2 kV, a buffer as thick as ~7 µm is reported [10] but this imposes several technological challenges. The wafer bow increases and therefore the wafers are prone to cracking [11]. This can hinder the epitaxial growth scaling over larger wafer sizes. Moreover, the need of thick buffer layers significantly increases the growth cost with reduced growth yield.

We have previously demonstrated that V_{BD} of GaN-on-Si DHFETs can be significantly enhanced by Si removal either via global or local Si removal schemes [6-8]. The scope of the present work is the realization of enhanced V_{BD} of GaN-on-Si DHFETs with optimized sub-micron thin AlGaN buffer after Si removal [6]. We present here for the first time that after Si removal, the buffer isolation test structures and devices breakdown voltages do not depend on buffer thicknesses because the path from source-to-drain across AlN/Si interface is interrupted. After Si removal [6], the buffer and the device V_{BD} show a linear increase as a function of ohmic gaps and gate-drain (L_{GD}) distances respectively. The electric field strengths are ~2.5 MV/cm and ~1 MV/cm for buffer and device respectively for different buffer thicknesses (600 nm, 1 µm, 2 µm). A V_{BD} of over ~ 2000 V is observed for an AlGaN buffer thickness of only 600 nm and with a L_{GD} of 20 µm. As a comparison, the maximum V_{BD} for a 2 µm thick AlGaN buffer is only 650 V for devices without removing the Si substrate. We believe that the growth of thin buffers on Si substrates, followed by Si removal, is a promising route to manufacture low cost high voltage GaN devices.

Layer Growth and Device Fabrication

DHFETs are fabricated starting from MOCVD grown $Si_3N_4/Al_{0.35}Ga_{0.65}N/GaN/Al_{0.18}Ga_{0.82}N$ hetero-structure layers on Si (111) substrates, with a thick *in-situ* Si_3N_4 cap layer. [12]. In our present study, 4 different $Al_{0.18}Ga_{0.82}N$ buffer thicknesses of 330 nm, 600 nm, 1 µm and 2 µm are grown. For all layers the thicknesses of the $Al_{0.35}Ga_{0.65}N$ barrier layer and the GaN channel are 25 nm and 150 nm respectively. For device processing, the following steps are executed: ohmic contact formation, device isolation (implantation), gate recess etching, Schottky-gate metallization and deposition of an interconnect layer. The fabricated buffer structures have varying ohmic gaps and DHFETs have source-gate distance L_{SG} = 1.5 µm, gate-length L_G = 1.5 µm, G-D distance L_{GD} = 5 - 20 µm and a total gate width W_G = 200 µm (Fig. 1).

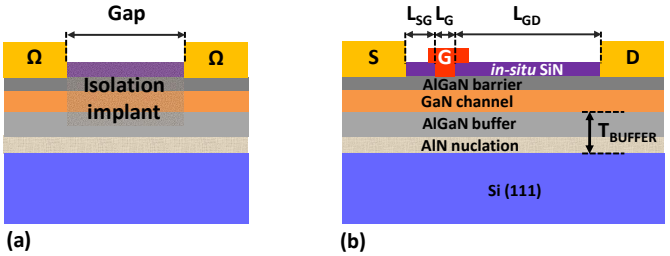

Fig 1. Schematic cross-sectional view of (a) a buffer isolation test structure and (b) a DHFET device. Ω = ohmic contact, T_{BUFFER} = total buffer thickness.

MEASUREMENTS AND RESULTS

The 2-DEG properties of the GaN channel are first characterized by Hall measurements before Si removal to study the layer qualities. Fig. 2 shows the Hall values: the sheet resistance (R_{SH}), mobility (μ) and sheet carrier concentration (N_S) as a function of AlGaN buffer thicknesses (T_{BUFFER}). It is evident that the 2-DEG channel properties remain identical for epilayers with the AlGaN buffer thickness down to 600 nm. However, significant channel degradation is observed for the 330 nm thick buffer [13-15].

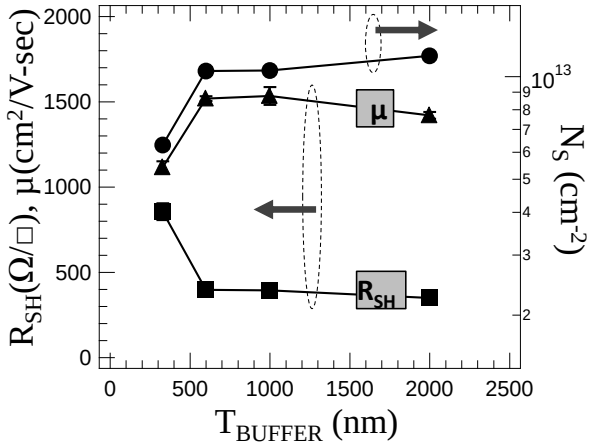

Fig. 2. Hall measurement for different buffer thicknesses.

The reduced N_S for the 330 nm thick buffer might result from enhanced electron trapping into electrically active acceptor like dislocations [14] and subsequently the μ drops due to enhanced 2-DEG channel scattering from the charged dislocations [15]. Typical I_{DS}-V_{DS} device characteristics with L_{GD} = 15 μm and with various T_{BUFFER} are shown in Fig. 3. The good quality of the channel layer is confirmed by the R_{ON} and the I_{DSAT} values for devices with 600 nm and 1 μm buffer (see Fig. 4 and Fig. 5).

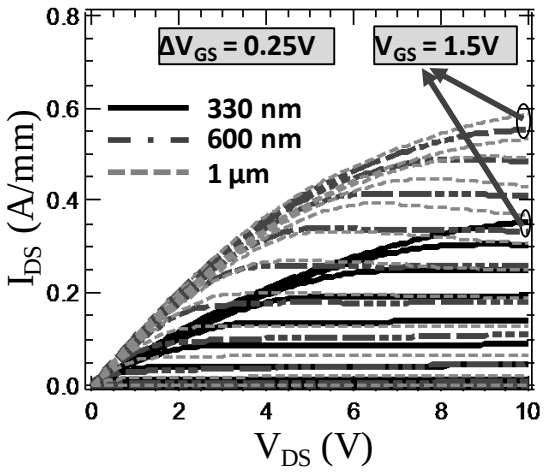

Fig. 3. I_{DS}-V_{DS} characteristics for different buffer thicknesses.

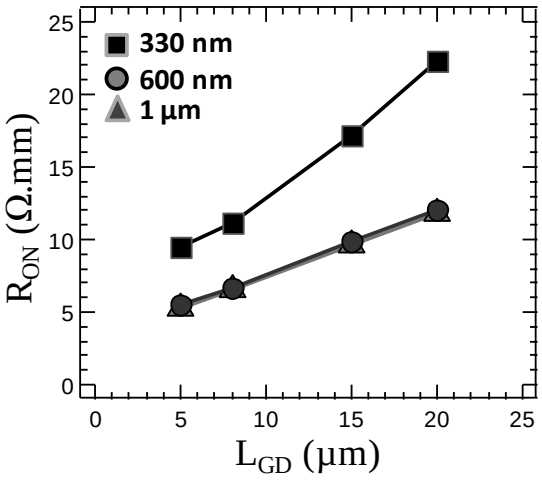

Fig. 4. R_{ON} versus L_{GD} at V_{DS} = V_{GS} = 1 V for different buffer thicknesses.

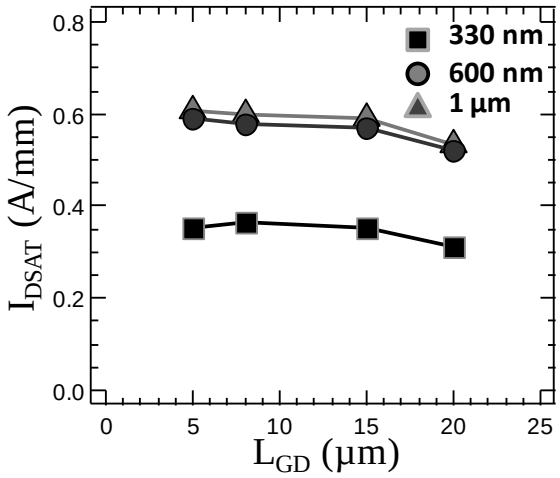

Fig. 5. I_{DSAT} versus L_{GD} at V_{GS} = 1.5 V and V_{DS} = 10 V for different buffer thicknesses.

From this, we can conclude that most of the dislocations (threading, screw or mixed) emanating from the AlN/Si interface are confined well within a buffer thickness up to 600 nm. Therefore, we will use T_{BUFFER} of 600 nm, 1 μm and 2 μm for Si removal study for V_{BD} enhancement.

V_{BD} for buffer isolation structures and devices is usually defined as the voltage at which the leakage current increases to 1 mA/mm. However, in case of the Si removal, a hard breakdown (which is marked as V_{BD}) is observed before a leakage current of 1 mA/mm is reached. We believe that the observed hard breakdown is related to the intrinsic breakdown of the III-N materials. Before Si removal, we observe a V_{BD} saturation at ~ 200 V, ~300 V and ~ 650 V for buffer thicknesses of 600 nm, 1 μm and 2 μm respectively for both buffer structures and DHFETs.

After Si removal, there is no V_{BD} saturation and a linear increase with ohmic gaps (see Fig. 6) and L_{GD} (see Fig. 7) is observed for both the buffers and DHFETs with electric field

strengths of 2.5 MV/cm and 1 MV/cm respectively. A DHFET breakdown measurement curve for L_{GD} = 20 µm is shown in Fig. 8 showing a V_{BD} of over ~ 2000 V. Therefore, after Si removal the V_{BD} is independent of the buffer thicknesses and is determined by the peak electric fields occurring in the structures (buffers and devices).

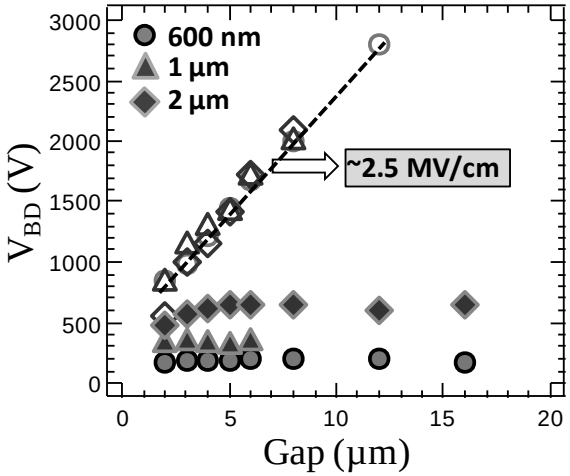

Fig. 6. Buffer V_{BD} versus ohmic gaps for different buffer thicknesses. Solid circles are V_{BD} with Si substrate and the corresponding open circles are measurement after Si removal.

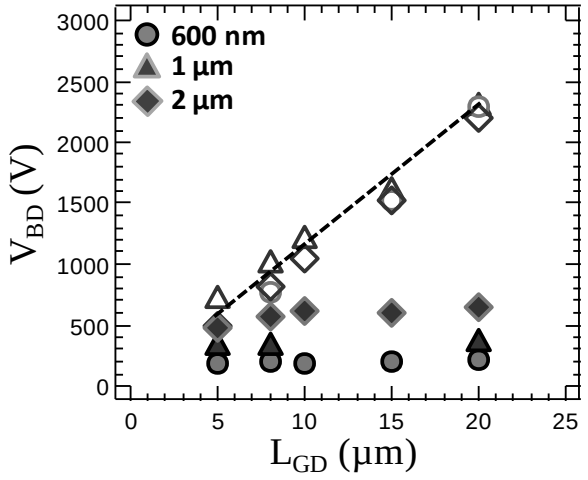

Fig. 7. (a) Device V_{BD} versus L_{GD} for different buffer thicknesses. Solid circles are V_{BD} with Si substrates and the corresponding open circles are measurements after Si removal.

Fig. 9 benchmarks the V_{BD} versus T_{BUFFER} data. It can be clearly recognized that very high V_{BD} devices (over ~ 2000 V) can be realized with much thinner buffer layers (~ 600 nm) after Si substrate removal compared to over ~ 7 µm thick buffers on the Si substrates having similar V_{BD}. Therefore, devices having thin buffers followed by Si substrate removal are promising solutions to obtain low cost, high yield and high manufacturability of high voltage GaN devices.

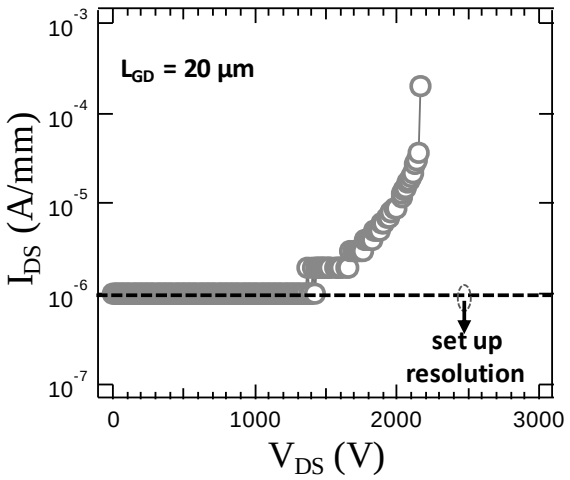

Fig. 8. A breakdown measurement curve (L_{GD} = 20 µm) after Si substrate removal with T_{BUFF} = 600 nm; showing a V_{BD} of over ~ 2000 V.

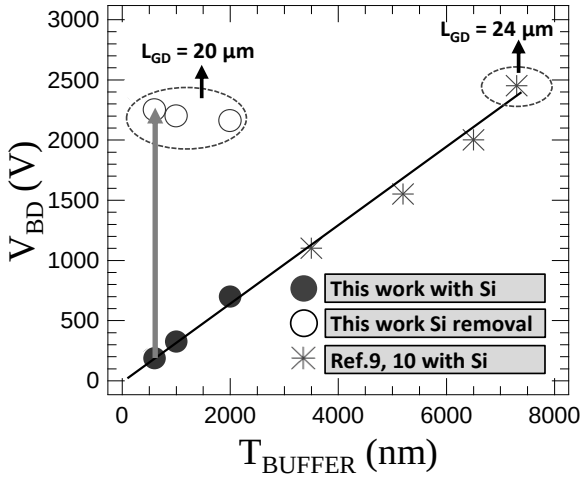

Fig. 9. Benchmarking V_{BD} versus buffer thicknesses.

CONCLUSIONS

We investigated GaN-DHFETs for different AlGaN buffer thicknesses with Si and after Si substrate removal. Thin buffer layers with a total thickness of 600 nm and above, showed good quality channel properties confirmed by the Hall measurements. We observed V_{BD} scaling trends before Si removal for 600 nm, 1 µm and 2 µm thick buffers. However, we found that after the Si removal, V_{BD} does not depend of the buffer thickness. We observed a V_{BD} of over ~ 2000 V for a L_{GD} of only 20 µm for a submicron buffer thickness of only 600 nm. A linear increase of V_{BD} as function of L_{GD} is observed with an average electric field strength of ~1.0 MV/cm. This confirms that the growth of

thin buffers combined with Si removal is one of the promising technological solutions to obtain low cost, high yield and high manufacturability of high voltage GaN devices.

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ACRONYMS

MOCVD : Metal Organic Chemical Vapor Deposition
2-DEG : Two Dimensional Electron Gas
DHFET : Double Hetero-structure Field Effect Transistor
T_{BUFFER} : Buffer Thickness
V_{BD} : Breakdown Voltage
L_{GD} : Gate-to-Drain Distance
µ : Mobility
N_S : Sheet Carrier Concentration
R_{SH} : Sheet Resistance