SESSION 11b: BACKSIDE PROCESSING / YIELD IMPROVEMENT

Chair: Travis Abshere, *TriQuint Semiconductor*

The session begins with a Skyworks Solutions discussion on a strategy for reducing GaAs wafer breakage that has worked well for them. Using a data driven approach and a cross functional team, they made a >90% reduction in breakage at grind – a traditionally high stress/high breakage rate processing step for GaAs. The second paper discusses Freescale's test vehicle for monitoring low occurrence die fractures in order to provide a monitor and method for improving manufacturing processes. The potential reliability risk from propagation of low occurrence die cracks missed at final test can be a thorn in the side of both manufacturers and customers. Paper three is a M/A-COM Technical Solutions topic concerning aspect ratios of GaAs backside vias. It builds on previous M/A-COM work for creating pillar free vias on low aspect ratio designs. This work explores the higher aspect ratio arena for a variety of critical parameters. The fourth paper is a TriQuint Semiconductor submission for reducing rework rates for wafers mounted to Si substrates for backgrind. Like the breakage reduction effort mentioned above, this was a collaborative effort among different groups to improve a process through multiple changes rather than a single large impact change. We "finish" out the session with a WIN Semiconductors presentation on improving yields for 50 µm GaAs products. Unlike the yield improvements above that were focused on breakage or cracking, this work takes a harder look at particle contamination and air bridge collapse, especially at the die plate step.