

SESSION 7a: NOVEL DEVICES

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This session has four exciting papers describing industry directions and novel approaches to future MOSFET fabrication using a variety of material systems, including Ge, various III-Vs and amorphous InGaZnO. The first paper is an invited talk which reviews the current status and future directions for III-V MOSFETs as a route to enabling continued scaling of CMOS at and beyond the 15 nm generation by utilizing the high channel mobilities offered by III-Vs. The scaling-driven requirement to reduce device pitch and ohmic contact size will force significant reduction in contact resistances for III-V ohmics to be used in this domain. The Si industry move, led by Intel, toward FinFET architectures for 22nm and below will also push any < 15nm III-V MOSFETs toward some non-planar technology.

The second paper describes an inverted InAlAs/InGaAs MOSFET fabricated with MOCVD re-grown source/drain ohmics and then deposition of the alumina gate dielectric by ALD. This approach eliminates the need for gate-recess etching and promises low on-resistance and high drain current with a smaller footprint than conventional recessed FETs.

The third paper describes inverted thin film transistors (TFT), fabricated on glass substrates with a Mo gate, a composite gate dielectric comprised of ALD deposited HfO₂ followed by sputtered SiO_x, and with channel of sputtered amorphous InGaZnO. These devices have shown impressively steep sub-threshold swing (SS) values of 96 mV/decade and on- to off-state current ratios of 1.5E10, which make them very promising for low voltage operation and low power dissipation ICs.

The fourth paper, which is also an invited talk, reviews the use of Ge and III-Vs grown on Si for the next generation of CMOS. The paper also describes challenges and directions in the choice of gate dielectrics for both Ge (SiGe) pFET and InGaAs nFET for sub-1nm EOT MOSFETs.