SESSION 8a: PROCESSING – GATES
Chair: Russ Westerman, *Plasma-Therm, LLC*

Papers in this section focus on gate formation and optimization in compound semiconductor device manufacturing. The first paper of the session by the Naval Research Laboratory discusses techniques to increase the yields of sub-quarter micron devices using a bi-layer resist approach to gate formation. The paper discusses the optimization of the resist process flow to facilitate gate formation and shows fabricated gate lengths near 40nm.

The second paper in the session from TriQuint Semiconductor describes the development and implementation of an optical lithography process to replace an existing 0.15 µm e-beam process. The paper will discuss the characterization of the optical lithography steps as well as comparing the performance of the optical and e-beam fabricated devices.

The third paper in the session is a collaboration between the University of Washington and TriQuint Semiconductor. This paper discusses the migration of an existing plasma process for gate recess etching to a high density inductively coupled plasma (ICP) etcher. Results from designed experiments used to screen and then map the new process space are presented.

The fourth paper of the session from WIN Semiconductors Corp examines issues related to stringer formation during gate metallization. Alternate cleaning methods using a combination of spray & soak techniques are explored in order to eliminate stringers without compromising the gate integrity.

The fifth paper in the session will also be presented by WIN Semiconductors Corp. This paper looks at productivity improvements to a 0.15 µm e-beam based T-gate process. This work looks at the optimization of the resist develop step. Through automation of the develop step, this group was able to increase the overall process yield while simultaneously reducing the overall process variability.

The last paper of the session, by the Shibaura Institute of Technology, examines the effect of adding field plates to GaAs MESFET devices in an effort to reduce gate lag and current slump. Using device modeling, the effects of different field plate configurations are explored in order to minimize the effect of surface states and bulk traps on device performance.