Yield Learning of a GaAs-Based High-Throw Count Switch for Handset Applications

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ABSTRACT:

In 2011, TriQuint introduced a new Dual-Band Transmit module to the handset market containing a GaAs-based high throw count switch [1, 2]. Initial pre-production yields were below expectations where the switch was found to be the cause. Stringent application-specific DC die sort test requirements, increased process complexity and switch design topology employing a high gate density were all factors in the depressed yield. Failure analysis showed that for the first time at TriQuint, an RF product was yield-limited due to process defects, rather than parametric variation. Reducing defects to enable high yield and reliability has long been critical for Silicon manufacturing, however, for GaAs manufacturing, parametric failures are often on top of the yield Pareto.

This paper will first outline the development of a DC die sort test methodology which not only assured high final test yield but also prevented test escapes due to limitations in the measurement of IMD2 and third-order Harmonics in the production test. Failure analysis results, which were integral to the discovery of a defect-driven yield loss mechanism, will be covered. As a preview, Figures 1 and 2 included here show a die sort wafer map of failing die and the ultimate root cause of the failure identified in a focused-ion beam cross-section in Figure 2. Additionally, sample die sort wafer maps showing identified patterns will be presented which helped drive the reduction of defects.

The paper will continue by discussing the systematic methodology used to identify sources of defects in the manufacturing process, including Automated Optical Inspection (AOI), line partitioning, best known methods, and the measurement of defect densities to predict yield improvement. Solutions driving the reduction of defect densities will be shared which were directly translated into switch die sort yield improvement.

KEYWORDS: AOI, GaAs, high-throw switch, defects, die sort, line partitioning, focused-ion beam, failure analysis

REFERENCES:

[1] C. Nevers, A. T. Ping, T. Rivers, S. Varma, F. Pool, M. Minkoff, E. Etzkorn, O. Berger, "High-volume 0.25um AlGaAs/InGaAs E/D pHEMT process utilizing optical lithography," *CS Mantech* 2009.

[2] M. D. Yore, C. Nevers., P. Cortese "High-Isolation Low-Loss SP7T pHEMT Switch Suitable for Antenna Switch Modules", 2010 EuMIC.

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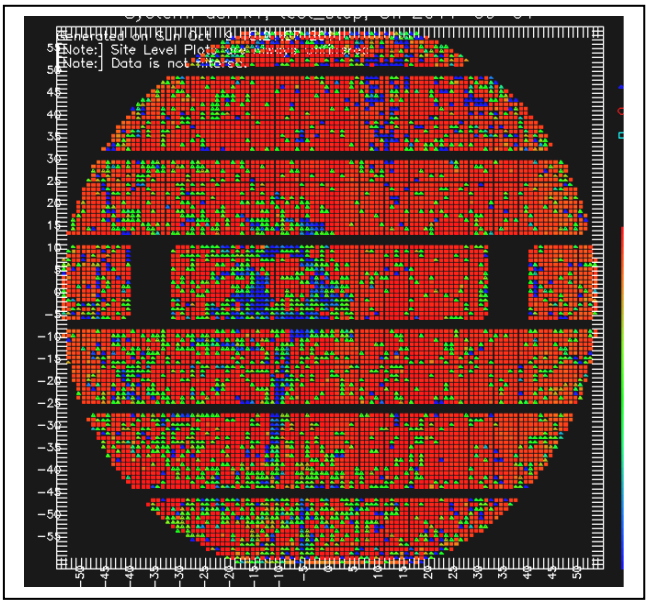

Fig 1: DC die sort wafer map showing die failing test. The failure pattern gave clues to the source of failures. Failing die were analyzed and a focused ion-beam (FIB) cross-section is shown in Fig 2.

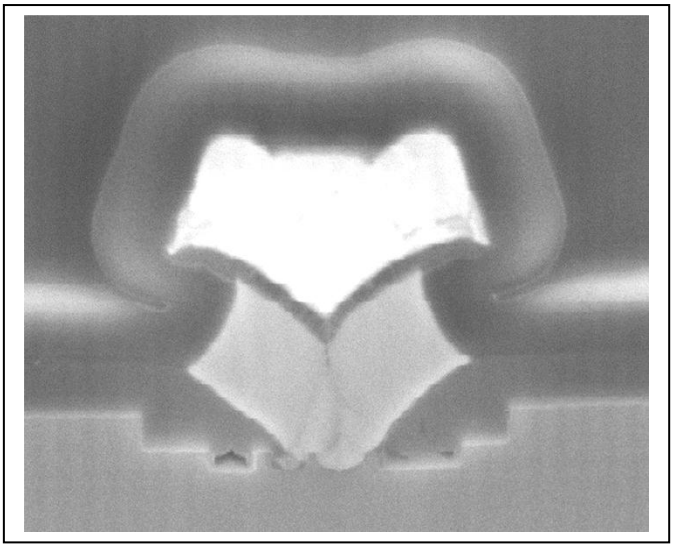

Fig 2: FIB cross-section showing root cause of the DC die sort test failures causing yield loss shown in the wafer map in Fig 1. Incomplete formation of the FET is observed causing excessive Drain off-current.