Crystal quality Improvement of epi-wafer for RF and power switching devices by growing VAS method of GaN substrates with low dislocation density uniformly distributed in a wafer

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Developments of GaN-HEMTs for high performance power devices has been struggling with non-liner effects like current collapse, drain lag and gate lag. Most of them are thought to come from various traps in the material, especially in the epi layers if the surface treatment process is fully matured. Origin of the traps can be divided into two groups; a) residual or doped impurities like Carbon, Iron and Oxygen and b) point defects like vacancies, interstitials, anti-sites and their complex. We reported about the behavior of Carbon and Ion by lights induced current method in the last conference[1)] and we can see some reports about these impurities[2)]. The role and character of the point defects, however, are totally not clear yet, because the GaN epi layers has too many defects (over E8-E10 cm-2), especially those on hetero-substrates like Si and SiC. To clarify this, we had experiments using the GaN substrates grown by VAS (Void Associated Separation) method, where defect density is quite low (< 3E6cm-2) and uniformly distributed across wafer both microscopically and macroscopically. This uniformity enables us to have stable and accurate characterization. The quality difference of epi-layer on SiC substrate and that on VAS-GaN substrates are discussed from view point of traps and potential device performance is demonstrated in this paper.

EXPERIMENTS & RESULTS

The high resistive buffer layers doped by carbon or iron were grown on SiC and GaN substrates under exactly same growth condition and the I-V curve under different color LED illuminations were measured. We didn't find any significant difference between SiC and GaN. The behavior seems to be dominated by doped impurity. Point defects can't be "main" items to determine the leakage. The control of impurity is necessary on this point. The influence of point defects on leakage itself seems to be minor, if any.

Then, GaN-HEMT structures on these substrates were grown. No significant difference was observed in the basic "major" properties like sheet carrier concentration and mobility. But PL profiles on GaN substrates showed very high band emission and lower so called "yellow peak" as shown in Fig.1, which is said to come from some unknown defects and affects the non-linear behavior of the transistors. This indicates lower density of point defects on GaN substrates has high possibility of device improvement.

Based on this results, the GaN p-n diode for power switching devices are fabricated using this VAS-GaN substrates, whose uniformity (no localized concentration of the defects) can help the stable performance of the devices with very large electrode more than 100 um diameter. The extremely high breakdown voltage over 3000V has been obtained from this device shown in Fig.2. This shows clear demonstration for using low and uniformly distributed defect density GaN substrate for performance improvement on GaN power devices.

REFERENCE

1)T.Tanaka et al.;Digest of CS-MANTECH 2012 (Boston) pp293

2)U.Honda et.al; J.J.A.P 51(2012) 4DF04

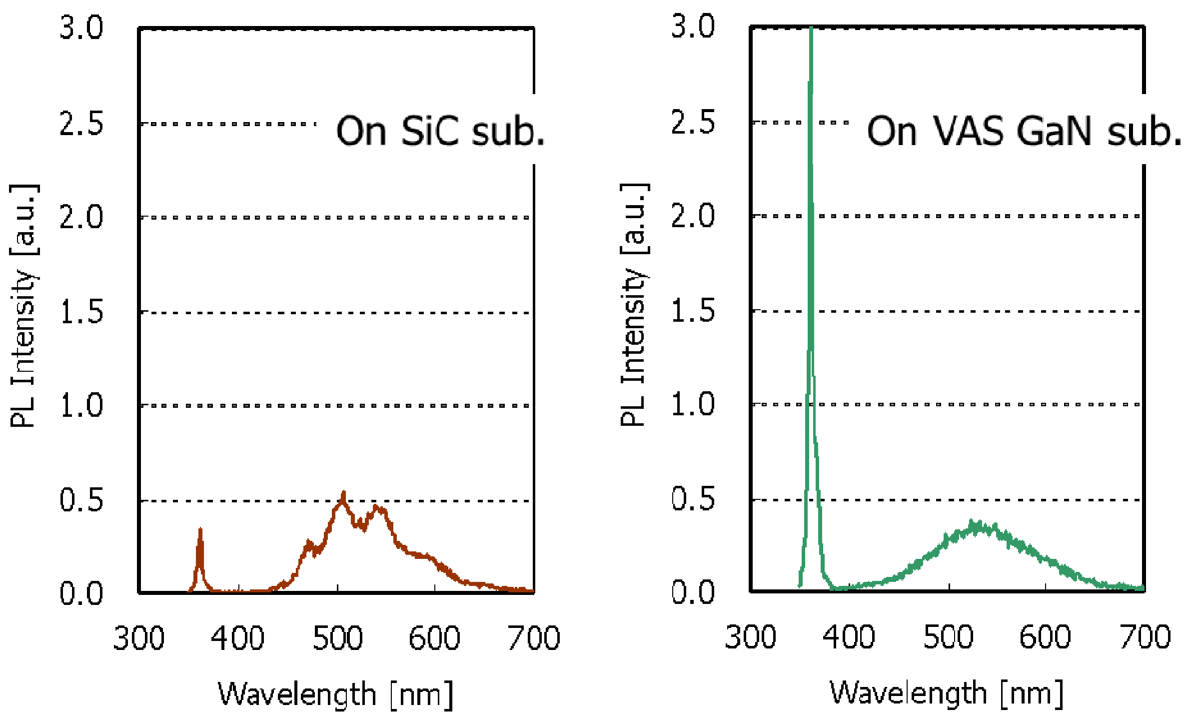
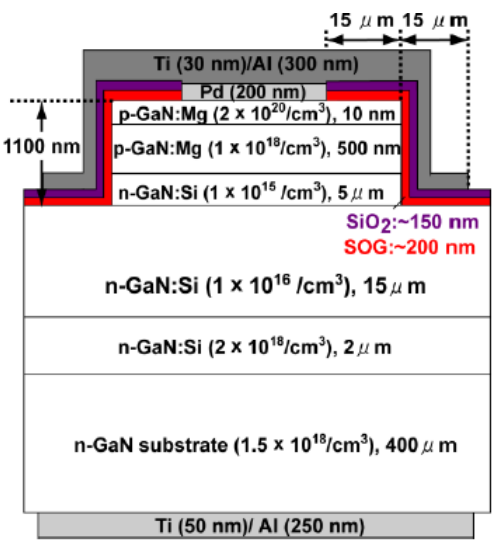
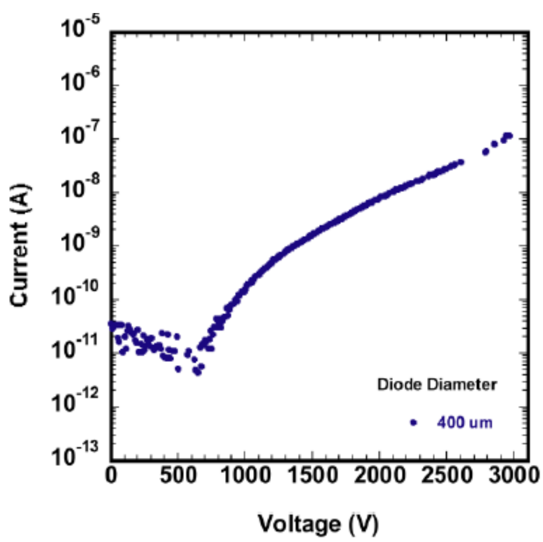


Fig.1 PL profile of GaN-HEMT-epi grown on SiC and GaN substrate by same growth condition



(a) Cross section of P-N diode



(b) Breakdown result

(b)

Fig.2 Over 3000V Breakdown of P-N diode grown on BAS GaN substrate