DARPA's Intra/Interchip Embedded Cooling (ICECool) Program

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Abstract

The Defense Advanced Research Projects Agency (DARPA) is currently pursuing research working toward a new paradigm of embedded cooling for thermal management of microelectronic device. This work was initiated in the Near Junction Thermal Transport (NJTT) thrust, which is the transitional effort to an embedded paradigm, building on the advanced remote cooling developed in the Thermal Management Technologies (TMT). The full implementation of embedded cooling is being pursued in the two efforts of the Intra/Interchip Enhanced Cooling (ICECool) program: ICECool Fundamentals and ICECool Applications.

BACKGROUND

The increased integration density of electronic components and subsystems, including the nascent commercialization of 3D chip stack technology, has exacerbated the thermal management challenges facing electronic system developers. The confluence of chip power dissipation above 100W, localized hot spots with fluxes above 1kW/cm^2, and package-level volumetric heat generation that can exceed 1 kW/cm^3 has exposed the limitations of the current "remote cooling" paradigm and its inability to facilitate continued enhancements in the performance of advanced silicon and compound semiconductor components. These thermal limitations have compromised the decades-long Moore's Law progression in microprocessor performance and threaten to derail the innovation engine which has been responsible for much of the microelectronic revolution.

In conventional cooling architectures for electronics, reliance on thermal conduction and spreading, in the commonly-used chips and substrates and across the multiple material interfaces present in packages and modules, severely constrains the ability of remotely located heat rejection surfaces to reduce the temperature rise of critical on-chip hot spots and individual chips in a module or in a stack. Moreover, continued application of this "remote cooling" paradigm, has resulted in electronic systems in which the thermal management hardware accounts for a large fraction of the volume, weight, and cost of advanced electronic systems and undermines efforts to transfer emerging electronic components to portable, as well as other small form-factor, applications.

THERMAL MANAGEMENT TECHNOLOGIES (TMT) PROGRAM

In 2008 DARPA initiated the Thermal Management Technologies (TMT) program to address these thermal management challenges by reducing the overall thermal resistance associated with the prevailing "remote cooling" paradigm. The TMT program includes several distinct efforts to utilize emerging micro- and nano-technology for enhanced thermal performance and these efforts are now coming to fruition, with considerable success [1].

The Microtechnologies for Air Cooled Exchangers (MACE) effort seeks to develop heat sinks which utilize flow agitators, synthetic jets, compressed air, and fins with integral heat pipes to reduce the thermal resistivity towards 10 cm^2 K/W, meaning a 10 Kelvin temperature rise for a heat flux of 1 W/cm^2, with a fan Coefficient of Performance (COP) approaching 30. The Thermal Ground Plane (TGP) thrust is developing high-performance "vapor chamber" heat spreaders in which micro-nano biporous wicks, some with hydrophobic-hydrophilic surfaces and expansion-matched cases, can provide in-plane thermal conductivities between 10kW/mK and 20kW/mK, or 25-50 times higher than copper and more than 10 times higher than synthetic diamond. Enhanced thermal interface materials, based on mechanically-compliant laminated solder-graphite, GLAD fabricated copper nanosprings, and arrays of Carbon Nano Tubes (CNT's), respectively, that could accommodate the differential expansion between silicon and copper while reducing the thermal resistivity to below 0.01cm^{2}K/W for a 0.1mm thick layer, are resulting from the NanoThermal Interfaces (NTI) thrust. Miniature high-efficiency refrigeration systems, based on thermoelectric or Sterling cycle technologies that can be inserted into the chip stack-up and capable of reaching COPs of 2 for a 15K temperature reduction under an applied heat flux greater than 25W/cm^2, are being pursued under the Active Cooling Module (ACM) effort.

NEAR JUNCTION THERMAL TRANSPORT (NJTT)

The Near Junction Thermal Transport (NJTT) thrust initiated DARPA's efforts in the creation of a new "embedded cooling" thermal management paradigm. NJTT is

attempting to reduce the thermal resistance of the near-junction region (the first 100 µm) of microelectronic devices, without producing deleterious effects in electrical performance. NJTT is thus establishing a dividing line between the limits of the current "remote cooling" paradigm and the emergence of an integrated, "embedded cooling" paradigm.

NJTT is focused on approaches that will allow GaN PAs to operate in existing DoD systems with significant increases in power handling and without accompanying increases in the temperature difference from the junction to the base of the heat sink or cold plate, deleterious effects on the electrical characteristics, or incompatibilities in material sets or fabrication processes. NJTT teams are not altering the electrical design of the PAs, but rather are pursuing thermal management approaches, such as high conductivity materials or liquid cooling, that can substantially reduce or remove the thermal barriers to high-power operation of GaN PAs and similar components.

NJTT, an 18-24 month program, began in late 2011.The specific teams and their approaches include the following. BAE Systems, Raytheon Integrated Defense Systems, RFMD, and TriQuint Semiconductor are exploring epitaxial transfer of GaN onto high conductivity diamond substrates. NGAS is exploring direct growth of diamond into vias etched in the SiC substrate of the GaN. The final NJTT team, GE Global Research, is exploring single-phase cooling of a GaN on SiC PA with microchannels etched into the SiC substrate within 50 µm of the GaN.

Additionally, NJTT has a strong focus in metrology and modeling to address the challenges of measurement verification at this scale and quantifying thermal and electrical performance of the GaN devices. At the end of the program, the teams will demonstrate the improved power handling of their techniques by incorporating them into test structures or existing GaN PAs.

INTRACHIP/INTERCHIP ENHANCED COOLING (ICECOOL)

DARPA's Intrachip/Interchip Enhanced Cooling (ICECool) program picks up where NJTT left off and is focused on fully implementing the new "embedded cooling" paradigm. ICECool will explore disruptive thermal technologies that will mitigate thermal limitations on the operation of military electronic systems, while significantly reducing size, weight, and power consumption (SWaP). The overarching vision for ICECool is to place thermal management on an equal footing with functional design and power delivery and utilize embedded thermal management to enhance the performance of military electronic systems.

ICECool will involve the creation of a rich micro/nano grid of thermal interconnects, using high thermal conductivity - as well as thermoelectric – materials to link on-chip hot spots to convectively and evaporatively cooled microchannels. Such intra/inter chip enhanced cooling approaches will need to be compatible with the materials, fabrication procedures, and thermal management needs of emerging homogeneous and heterogeneous integration in 3D chip stacks, 2.5D constructs, and planar arrays. An *intrachip* approach would involve fabricating micropores and microchannels directly into the chip [2, 3] while an *interchip* approach would involve utilizing the microgap between chips in three-dimensional stacks [4], as the cooling channel. In addition to the inclusion of an appropriate grid of passive and/or active thermal interconnects, it is expected that a combination of *intrachip* and *interchip* approaches, linked with thru-silicon and/or "blind" micropores will confer added thermal management functionality. These microchannels and/or micropores will need to be integrated into a fluid distribution network, delivering chilled fluid to the chip or package and extracting a mixture of heated liquid and vapor to be transported to the ambiently cooled radiator. Moreover, on-chip microvalves – thermostatically or digitally controlled- will be needed to regulate the flow of the coolant and assure the most efficient use of its latent and sensible cooling capacity.

The ICECool program consists of two related thrusts: ICECool Fundamentals and ICECool Applications. The goal of ICECool Fundamentals is to demonstrate chip-level heat removal in excess of 1 kW/cm^2 heat flux and 1 kW/cm^3 heat density with thermal control of local submillimeter hot spots with heat flux exceeding 5 kW/cm^2, while maintaining these components in the usually-accepted temperature range of the chosen candidate application by judicious combination of intra- and/or interchip microfluidic cooling and on-chip thermal interconnects. ICECool Fundamentals is, thus, the first step toward achieving the system performance goals of the ICECool program and will develop the fundamental building blocks of intrachip and interchip evaporative microfluidic cooling. The goal of ICECool Applications is to utilize the intrachip and interchip technologies developed by the Fundamentals to close the gap between chip-level heat generation density and system-level heat removal density in high-performance electronic systems, such as computers, RF electronics, and solid-state lasers, and in doing so realize dramatic gains in performance of these systems.

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