Palladium Diffusion Barrier Grown by Electoplating for Backside Cu Metallization of GaAs devices

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Abstract

In the GaAs/Ni-P/Pd/Cu structure, the thermal stability of thin films has been investigated using SEM, XRD and sheet resistance measurement. Microstructural analysis by XRD indicated that the Pd electroless plating film changed from an amorphous structure to a polycrystalline structure by annealing. We successfully improved thermal stability of the Ni-P/Pd/Cu films by using the Pd electroplating with a crystalline adjuster. The lifetime of these films were estimated to be 1.6×10^8 hours at 125 ºC. To our knowledge, these results demonstrate for the first time that the Ni-P/Pd/Cu plating films are highly uniform and highly thermally stable and can be used in backside Cu metallization of GaAs devices.

INTRODUCTION

Comparing to the commonly used Au metallization for GaAs devices, Cu has a lower resistivity, a higher thermal conductivity and a lower cost. Therefore, the concern with Cu metallization has been growing for the recent years. We are concerned with the backside Cu metallization, as an alternative to Au metallization, through via-holes on GaAs substrates. The fabrication of the Cu diffusion barrier layer is one of the important issues for the use of Cu as the metallization metal. Ta-based materials deposited by the physical vapor deposition are currently an effective diffusion barrier for the Cu metallization in Si-ULSI technology [1]. However, these materials are not necessarily useful as backside Cu diffusion barrier in GaAs devices, since the via-holes of GaAs substrates etched by BCl_3/Cl_2 plasma have the high surface roughness which is difficult to cover the entire range of the via-holes.

We have focused on the plating film with excellent coatability, in particular, on the Pd plating film which has been used as Ni and Cu diffusion barrier layer in printed wiring board and package substrate [2]. In consequence, we have successfully solved these issues and the approaches are depicted in this article.

PALLADIUM ELECTROLESS PLATING

Polished 4-inch (100) GaAs wafers with 625 µm thickness were used. The Ni-P/Pd/Cu films are formed on the GaAs wafers. The Ni-P/Pd films are deposited by the electroless plating and, the Cu film is deposited by the electroplating, respectively. The Pd film is Cu diffusion barrier. The Ni-P film fulfills a dual role as an adhesion layer between GaAs and Pd and as an inhibitor for the formation of GaAs-Pd alloy. Additionally, the antioxidant layer is formed on the Cu surface. Figure 1 shows sheet resistivity of the sample as a function of annealing time at 270ºC and 300ºC.

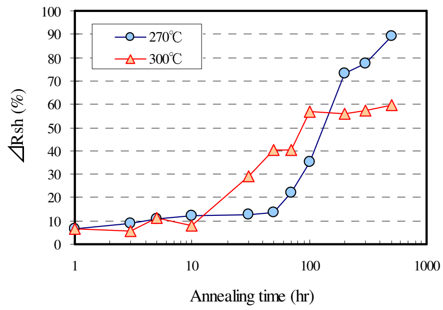
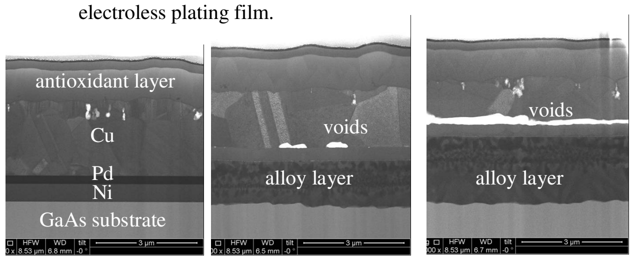


Figure 1. Sheet resistivity of the GaAs/Ni-P/Pd/Cu structure as a function of annealing time at 270ºC and 300ºC. The Pd film is the electroless plating film.

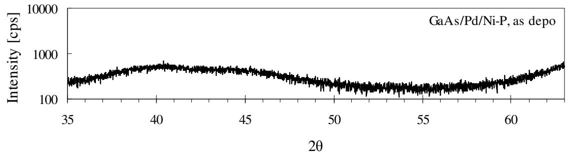


(a) as-deposited (b) after annealing for 100 hours at 270ºC (c) after annealing for 500 hours at 270ºC

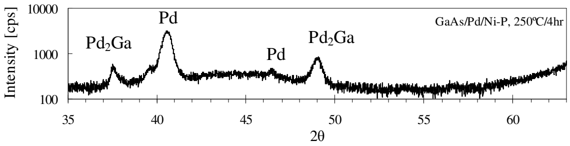
Figure 2. Cross section SEM images of the GaAs/Ni-P/Pd/Cu structure. The Pd film is the electroless plating film.

The sheet resistance is most affected by Cu film with the lowest resistivity of GaAs/Ni-P/Pd/Cu structures. The increase of ΔR_{sh} indicates that the Cu film thickness decreased due to Cu diffusion. Figure 2 shows the SEM image of the samples before and after annealing. After annealing, the alloy layer was formed between layers of Ni-P and GaAs. Cu was detected in the GaAs substrate by AES, which indicates that Cu exceeded Ni-P/Pd films and diffused into the GaAs substrate. It should also be added that Kirkendall voids are observed at the interface between the Cu film and the Pd film. These voids lead to the adhesive degradation between the Pd film and the Cu film.

Figure 3 shows XRD patterns of GaAs/Pd/Ni-P structure before and after annealing for 4 hours at 250ºC. XRD patterns indicate clearly change from a broad peak to some sharp peaks. This reveals the phase transition from amorphous to polycrystalline after annealing. These peaks are identified as Pd and Pd_2Ga peaks [3, 4]. The polycrystallization of Pd film leads to a high density of grain boundaries and, consequently, to the formation of fast diffusion paths which is disadvantageous for an application as a diffusion barrier.



(a) as-deposited



(b) After annealing for 4 hours at 250℃

Figure 3. XRD patterns of the GaAs/Pd/Ni-P structure

PALLADIUM ELECTROPLATING

It has been known that the microstructure of polycrystalline films was sensitive to the thermal stability and that the films with large grain size had higher resistance to the Cu diffusion [5]. To improve the barrier properties of the Pd films, we fabricated the Pd films by the electroplating. It is expected that the Pd electroplating films have larger grain sizes than the Pd electroless plating films.

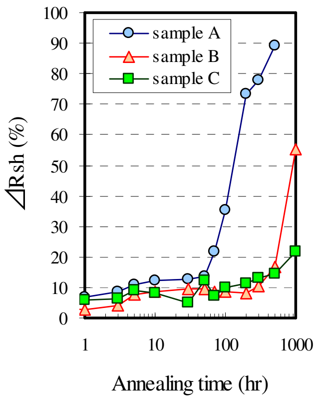
Samples A, B and C consisted of the GaAs/Ni-P/Pd/Cu structure. As shown in TABLE I, Pd films of samples A, B and C were deposited by the electroless plating, the electoroplating without a crystalline adjuster and the electroplating with a crystalline adjuster, respectively. The crystalline adjuster is a semimetal compound.

Figure 4 shows sheet resistivity of samples A, B and C as a function of annealing time at 270 ℃ and 300 ℃. Among the three samples after annealing, the order of increasing ΔR_{sh} was found to be in the sequence of sample A > sample B > sample C. The result clearly shows that the electroplating films have higher thermal stability than the electroless plating film. As shown in Figure 5, little Cu diffusion as illustrated by Kirkendall voids was observed in the Cu film of sample C after annealing for 1000hours at 270 ℃. After annealing for 500hours at 270 ℃, the Cu diffusion was stopped into the Pd film and Cu was not detected in the GaAs substrate by AES. In this thermal condition, ΔR_{sh} of sample C was 15 %. Therefore, assuming that the lifetime of the films was the annealing time at ΔR_{sh} = 15 %, the lifetimes were calculated using Arrhenius equation. The lifetimes of samples A and C were estimated to be 4.6×10^5 hours and 1.6×10^8 hours at 125 ℃, respectively.

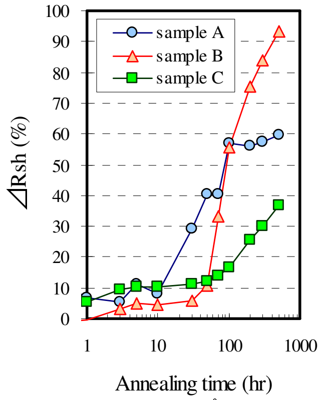
The reason for improvement of thermal stability by a crystalline adjuster is not clear yet. Further research on the correlation between the microstructure and barrier properties of Pd films would clarify the effect of a crystalline adjuster.

TABLE I
The differences of Pd formation methods

Sample	Pd plating method	Crystaline adjuster
A	Electroless plating	None
B	Electro plating	None
C	Electro plating	Semimetal compound

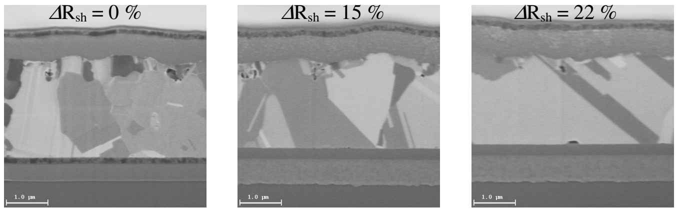


(a) at 270°C



(b) at 300°C

Figure 4. Sheet resistivity of samples A, B and C as a function of annealing time at 270℃ and 300℃.



(a) as-deposited (b) after annealing for 500 hours at 270℃ (c) after annealing for 1000 hours at 270℃

Figure 5. Cross section SIM images of sample C. The Pd film of sample C is the electroplating film with a crystalline adjuster.

CONCLUSIONS

In a GaAs/Ni-P/Pd/Cu structure, we found that electroless plating film changed from an amorphous structure to a polycrystalline structure by annealing. We successfully suppressed the Cu diffusion into the GaAs substrate by using a Pd electroplating with a crystalline adjuster. To our knowledge, results in this study demonstrate for the first time that the Ni-P/Pd/Cu plating films are highly uniform and highly thermally stable and can be used in backside Cu metallization of GaAs devices.

REFERENCES

[1]Rene Hubner, *Advanced Ta-Based Diffusion Barriers for Cu Interconnects*, Nova Science Publishers (2008)
[2] T. Totsuka, J. Surf. Finish. Soc. Jpn. **55,** 926 (2004)
[3] S. V. Nagender Naidu et al., J. Appl. Phys., **42**, 4971 (1971)
[4] J. O. Olowolafe, J. Appl. Phys., **50**, 955 (1979)
[5] M.Moriyama, Thin Solid Films, **416**, 136 (2002)

ACRONYMS

XRD: X-Ray Diffraction
AES: Auger Electron Spectroscopy
SEM: Scanning Electron Microscope
SIM: Scanning Ion Microscope