Recent Defense Production Act Title III Investments In Compound Semiconductor Manufacturing Readiness

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Abstract

In recent years, the Defense Production Act Title III program has invested in several projects to increase the manufacturing readiness level (MRL) of compound semiconductor MMIC power amplifiers (PAs) for radar and electronic warfare (EW) applications. This paper provides an overview of the Defense Production Act Title III, the benefits and risks associated with adopting GaN and ALD technology for radar/EW systems and the approach that Title III projects are employing to mitigate those risks.

This paper discusses the government management approach taken on four (4) Title III projects to improve the producibility and reliability of compound semiconductors. Each of the four participating Title III partners will submit separate papers and presentations that provide greater insight into their technical approach and accomplishments. All of the projects except for one, address GaN production. The atomic layer deposition coatings project is specific to GaAs.

INTRODUCTION

Since 2007, Title III has invested in 4 projects to improve the producibility of compound semiconductors:

1. Atomic Layer Deposition (ALD) Hermetic Coating for Microelectronics – Raytheon IDS
   - Environmental coating of GaAs MMICs
2. GaN on SiC X-band MMIC Production – Raytheon IDS
   - X-Band
3. GaN on SiC Radar/EW MMIC Production – Cree
   - S-Band and 6 – 18 GHz wideband
4. GaN on SiC Radar/EW MMIC Production - TriQuint
   - S-Band and 6 – 18 GHz wideband

The primary objective of each of these projects is to instantiate a production capability with a MRL of 8 which means that the process is ready for low rate initial production (LRIP) in a DoD acquisition program.

TITLE III DEFENSE PRODUCTION PROGRAM

The Title III Program is a Department of Defense-wide initiative under the Office of the Deputy Assistant Secretary of Defense for Manufacturing & Industrial Base Policy (MIBP). The Air Force serves as the Executive Agent for the Title III Program within the Department of Defense. The Title III Program Office, located at Wright-Patterson AFB, Ohio, is a component of the Manufacturing Technology Division of the Air Force Research Laboratory.

As outlined in Title III of the Defense Production Act of 1950, the mission of the DPA Title III Program is to create assured, affordable, and commercially viable production capabilities and capacities for items essential for national defense. This crucial mission is accomplished by support of these program objectives:

- Create, maintain, expand, protect, or restore the production capabilities of domestic suppliers whose technologies and products are critical to the nation's security
- Increase the supply, improve the quality, and reduce the cost of advanced materials and technologies
- Reduce U.S. dependency on foreign sources of supply for vital materials and technologies; and
- Strengthen the economic and technological competitiveness of the U.S. defense industrial base.

Title III promotes production capabilities that would otherwise be inadequate to support the material requirements of defense programs in a timely and affordable manner. Title III focuses on materials and components that could be used in a broad spectrum of defense systems. The direct and indirect benefits to defense programs resulting from Title III initiatives are substantial. Moreover, Title III projects create

numerous economic and technological benefits for domestic industries and consumers.[1]

ALD: Benefits/Performance

Integrating conformal atomic layer deposition into the wafer fabrication process enables environmental protection of MMICs at lower cost than with the extant hermetic packaging technology.

Existing silicon nitride (SiN) coatings were replaced with two types of ALD coating, performing all of the functions of the silicon nitride coatings plus providing resistance to humidity. Lower dielectric loading and better FET performance was achieved by substituting the ALD coatings for the SiN coatings rather than adding an additional environmental protection layer on top of wafers fabricated with the old SiN processes. The consistency of the deposition process resulted in tighter tolerances on capacitors and less variation in the RF properties of the FETs.

GaN PAs: Benefits/Importance

Phased array antennas are typically used for new DoD radar and electronic attack (EA) programs. Modern phased arrays typically utilize MMIC power amplifiers at each antenna element in the array that drive key radar and EA attributes including radiated power, prime power and cooling. The PAs also indirectly drive system cost and weight. GaN PAs have demonstrated significant benefits through DARPA programs in output power, DC power consumption (efficiency) and bandwidth vice conventional solid-state PA technologies.

GaN PAs: Manufacturing Risks

Mature PA fabrication often is a significant system-level factor for development and production schedules. PA fabrication often requires greater than 1 year during development and production. PA cost is often significant in system production. GaN PA manufacturing processes, in general, are relatively immature compared to production GaAs PAs. Production immaturity increases likelihood of:

- Rework or scrap during PA processing and associated significant system-level cost and schedule impact
- Variability and defects in PA product with associated yield loss/cost and potential for latent defects/failures.

Manufacturing Risk Mitigation through Title III

Title III programs are structured in three phases:

Phase I: Baseline Manufacturing Readiness Assessment. Significant quantities of wafers are manufactured to assess baseline process capability and yield. The baseline wafers provide data to identify root cause for variability and defects affecting yield, cost and schedule.

Phase II: Improvement and Refinement of Processes. Employing six sigma methodologies, successive designed experiments are conducted to reduce product variability and defects. A related objective is to improve screening criteria to assure reliable life-time operation.

Phase III: Final Manufacturing Readiness Assessment. Significant quantities of wafers are produced to assess final process capability and yield. This final assessment serves is critical to demonstrating to DoD acquisition programs the maturity of the process. The goal of these Title III programs is to establish a MRL of 8 (ready for LRIP).

Conclusions

GaN PAs have demonstrated significant performance benefits for DoD radar and EA systems through DARPA programs. However, GaN PAs introduce development risks due to relatively immature manufacturing processes. These risks are being mitigated through Title III projects. The GaN projects are successfully targeting and achieving reduced PA process variability and defects to improve yield/cost and reliability.

Equally important is reducing system manufacturing and integration costs of radar elements employing these advanced MMIC components. Significant cost reductions have been achieved in this area by improving dielectric and environmental coatings using ALD techniques. Application techniques, process maturation, and performance improvements are also being achieved under these Title III programs.

References

[1] DPA Title III Brochure, 2012, Manufacturing & Industrial Base Policy

Acronyms

ALD: Atomic Layer Deposition
DARPA: Defense Advanced Research Projects Agency
DoD: Department of Defense
FET: Field Effect Transistor
GAO: Government Accountability Office
GaAs: Gallium Arsenide
GaN: Gallium Nitride
LRIP: Low Rate Initial Production
MIBP: Manufacturing Industrial Base Policy
MMIC: Monolithic Microwave Integrated Circuit
MRA: Manufacturing Readiness Assessment
MRL: Manufacturing Readiness Level
SiC: Silicon Carbide
SiN: Silicon Nitride