Evaluation of Material and Process Contributions to BiFET Variation Using Design of Experiments

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During the modeling and characterization of FETs in our BiFET process [1], we performed a number of experiments to explore process variation of the FET parameters, in particular Idss and V_p. These included various experiments on material parameters, etch tools, and gate metallization. We observed that plots of Idss vs. V_p^2 for all of these experiments follow approximately the same line, shown in Figure 1 – the details of the experiments will be shown in the presentation. Where Idss is the zero gate bias current and V_{p2} is the pinch-off voltage (defined as the voltage at which Id=2.5%*Idss is obtained). The variation of Idss and V_p along this line is readily included in compact models for circuit simulation [2]. This behavior of Idss-V_p^2 is not unique to BiFET and can be observed by plotting the data from [3] and [4] as shown in Figure 2.

However, over large volumes of data, there are points that deviate from this line. The broadening of the data along this line (so that the data different from the expected behavior) cannot be simply modeled. To determine the possible causes for this, we laid out an experiment where we varied the FET layout (gate length, gate width, and channel width – defined in Table 1) and measured key FET performance parameters. In analyzing this data, we found that the best way to visualize it was to calculate the distance of the Idss-V_p^2 point from this line (this essentially amounts to rotating the coordinate system). The results of this transformation are shown in Fig. 3 along with the Idss variation. States marked with 1 are at the 3 sigma limit for that parameter and 2 is 6 sigma. The results allow us to clearly determine the influence of each of these parameters in making the devices "non-ideal." More importantly, we see combinations of factors can cancel. For comparison, the variation in Idss only is also shown in this figure. This method can be applied to other FET technologies to gain a better understanding of how material impacts the FET Idss versus the process.

The details of the comparison and some further analysis will be presented in the full abstract.

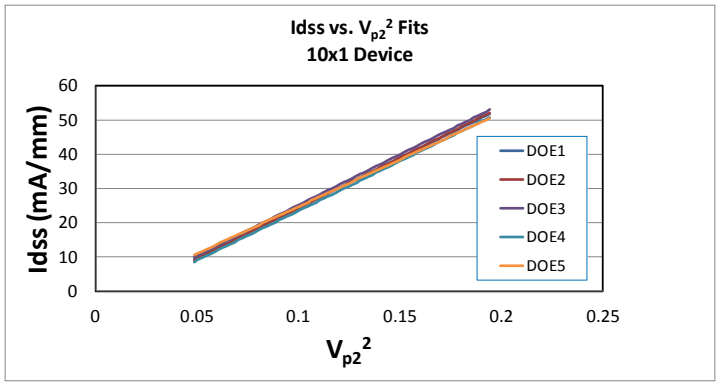
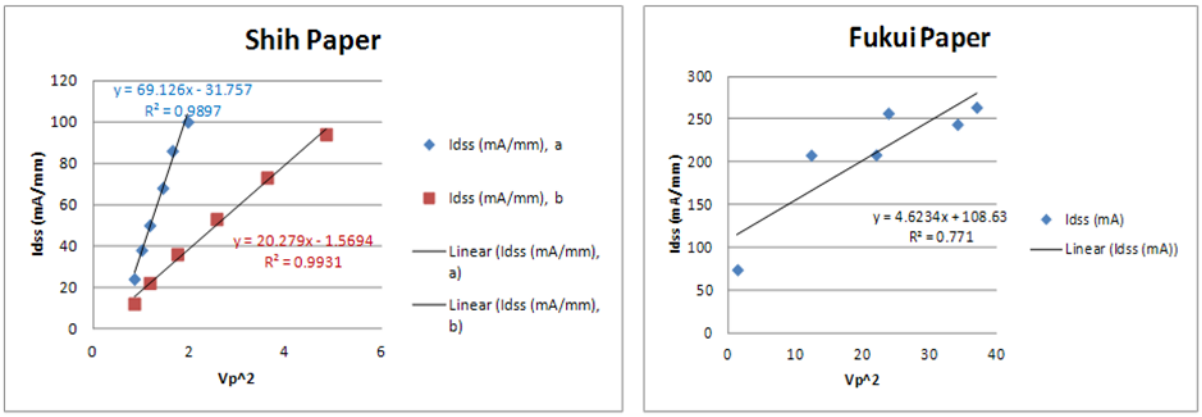


Fig. 1 Resulting Linear Fit from Various Material Designs of Experiment (DOEs)

W	CH	L	Point
- -	- -	0	-2_-2_0
-	-	0	-1_-1_0
- -	+ +	0	-2_+2_0
-	+	0	-1_+1_0
+ +	- -	0	+2_-2_0
+	-	0	+1_-1_0
+ +	+ +	0	+2_+2_0
+	+	0	+1_+1_0
0	0	0	0_0_0
0	-	-	0_-1_-1
0	+	-	0_+1_-1
0	-	+	0_-1_+1
0	+	+	0_+1_+1

Table 1. Description of DOE State for Experiment



(a) Power device (b) Low Noise Device. Gaussian Profiles Simulating Gate Etch Varied Doping (N), Active Channel Thickness (a) , Length (L), Width (Z)

Fig. 2. Idss vs. Vp^2 for Examples from Literature

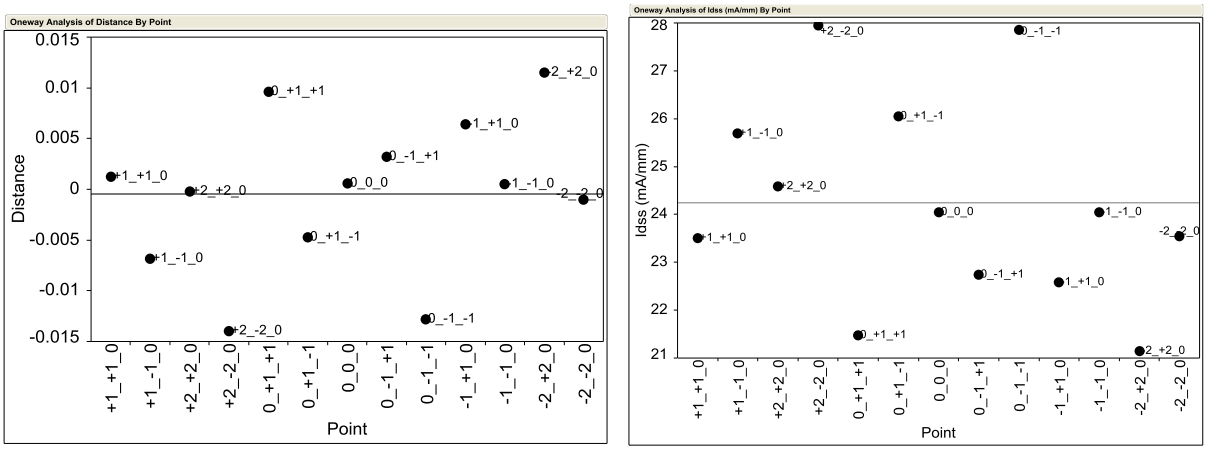


Fig. 3. Resulting distance from Idss-Vp2 fit line for different DOE states and the resulting Idss variation by state.

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