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Back Metal Optimization for PbSn Die Attach Assembly

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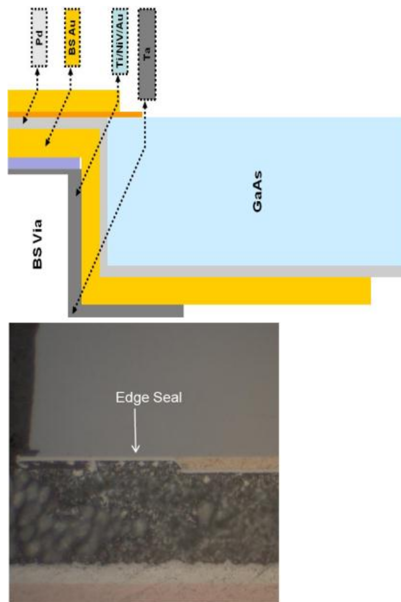
Abstract

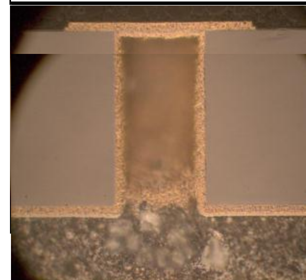
During qualification of a GaAs RF Power Amplifier we encountered die bond voiding issues using an existing backside metal stack process and assembly method. The problem manifested when the process was run at different Fab. The process was transferred using a copy smart approach where the thicknesses were matched but processing tools were different. During the pre-qualification process, die voiding issues were encountered not meeting manufacturing indices specs, and pre-qualification reliability failures were encountered. Experiments were run to optimize the back metal stack to achieve passing die bond criteria specs and reach manufacturability. In addition, reliability was validated by using JEDEC standard battery of tests on the optimized process.

Introduction

Freescale utilizes a metal stack specialized for high power GaAs PA which are assembled using PbSn based soft solder (CS MANTECH Conference, April 24-27, 2006, Vancouver, British Columbia, Canada).



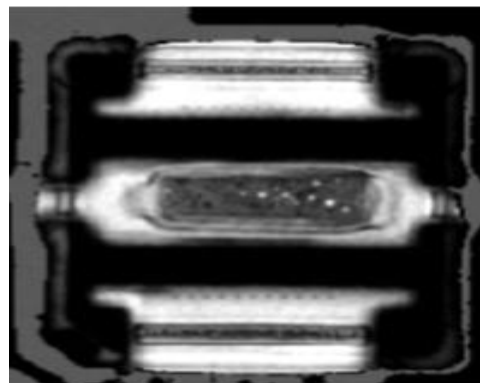
Starting from GaAs and working toward the back side surface, the traget flat films:
1- Pd
2- Au plated then street etch
3- Ti sputtered
4- NiV sputtered
5- Au sputtered
6- Au plated
7- Ta sputtered then liner etch - Ta insdie Via
8- Laser dicing



The process was transferred to a different Fab. The shown metal stack was duplicated at the new Fab but processing tools were not identical to original Fab. This required validation of the new process using assembly process indices and JEDEC standard reliability testing. Special attention was paid to die bond coverage which plays an important reliability role. Die bond coverage has been, historically, a key factor to maintain reliability and Freescal's high quality standards.

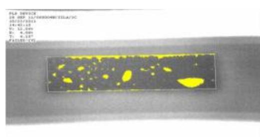
Initial results during pre-qualification showed acceptable die attach during assembly characterization and passed basic reliability testing (MSL + Temp Cycles and MSL + THB), results are shown below.

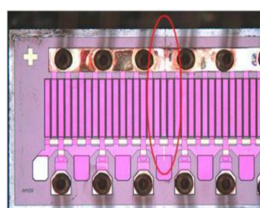
Unit	VOID % (SPEC 5%)		
	Total (Lot1)	Total (Lot2)	Total (Lot 3)
1	1.57%	2.80%	2.37%
2	1.12%	1.57%	2.29%
3	0.91%	1.68%	1.18%
4	2.16%	1.38%	1.91%
5	1.26%	1.71%	2.04%
6	1.03%	0.52%	1.58%
7	0.54%	1.07%	0.57%
8	2.14%	0.67%	1.51%
9	1.76%	0.24%	0.53%
10	1.38%	0.25%	1.48%
MIN	0.54%	0.24%	0.53%
MAX	2.16%	2.80%	2.37%
AVE	1.39%	1.19%	1.55%
STDEV	0.53%	0.80%	0.64%
Cpk at 5%	5.451	3.658	4.375



Process Optimization

Further recipe optimizations for manufacturability readiness manifested issues in meeting die attach criteria. Excessive die attach voiding and mechanical failures during reliability testing in the form of die cracks were observed, see results below.

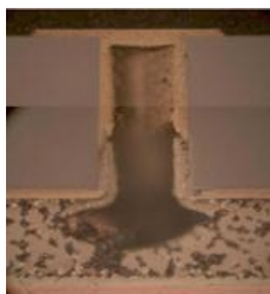




Parts	Total VOID % (SPEC < 5%)
1	5.00
2	6.41
3	12.06
4	7.37
5	9.29
6	11.45
7	8.54
8	6.76
9	9.59
10	10.41

Au Plating process control was not sufficient to eliminate the assembly and reliability failures. Plated Au thickness showed too much variation which impacted the formation of a good inter metallic interface. A switch from plated Au to sputtered Au was required to achieve repeatable thicknesses control. But we still encountered excessive voiding as seen with the original process.

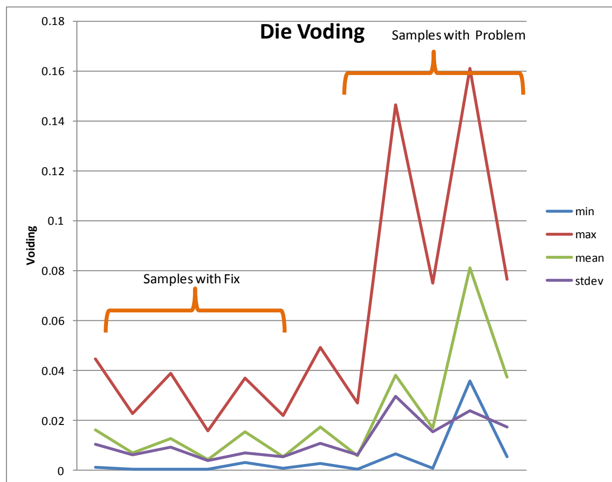
In order to understand the root cause of the excessive voiding we performed SEM cross sectional analysis and AFM. Previous results

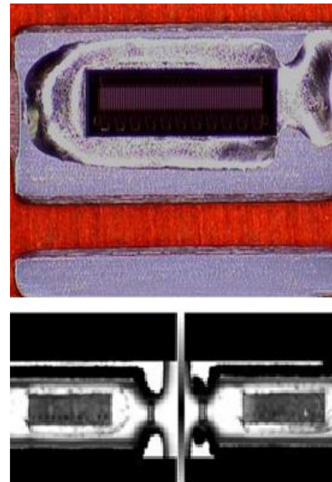


which led to the change from plated Au to sputtered Au indicated that thicker Au produced more voiding. The volume ratio of Au to Sn must be controlled to prevent formation of brittle $AuSn_4$ inter metallic that is known to cause reliability failures. SEM cross section of the sputtered Au did not show abnormal thickness. AFM analysis showed that the sputtered Au grains were smaller and more densely packed. But the voiding was still present. The sputtered gold (Au) sacrificial layer (Ti/NiV oxidation protection) was too thick causing malformation of the die bond IMC. The abnormal structure is very brittle as shown in the cross-section. Experiments were run at Fab and assembly to determine the main process variables. Die attach process DOEs, and Fab metal deposition and thickness splits were generated to understand the main effects. After several iterations it was discovered that the plated Au layer was unnecessary and that a thin layer of sputtered Au was sufficient to protect the Ti/NiV and be consumed efficiently during the PbSn reaction to form a good die bond.

Results

Sputtered Au processing is much more controllable to yield thin layers. Good die bond and successful reliability testing were achieved after optimizing the Au sacrificial layer to minimize volume and prevent reaction with PbSn soft solder.





Conclusion

The back metal Au sacrificial layer has to be controlled well to prevent excessive volume from reacting with PbSn soft solder during the die attach. Formation of unwanted die bond inter metallics can impact the quality of the die attach as well as the reliability of the device due to the brittle nature of bond and the susceptibility of GaAs to cracks. The challenge was to identify the root cause, knowing that the original metal stack was a proven process, and recognizing that the extra Au is actively reacting with PbSn due to the excessive volume. A thin layer of sputtered Au was sufficient to protect the Ti/NiV from oxidation and to be consumed efficiently during the PbSn reaction to form a good die bond. Qualification and process validation were performed successfully achieving release to production.

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