Formation of slanted gates for GaN-based HEMTs by combined plasma and wet chemical etching of silicon nitride

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A commonly used technology sequence in the fabrication of GaN-based HEMTs and MMICs is the so-called "embedded gate" process, in which the gate metal is deposited into a trench opening in a dielectric passivation layer usually consisting of silicon nitride (SiN_x). Control of the trench etching is of great importance, as the later semiconductor-metal interface at its bottom contributes significantly to the electrical characteristics and the reliability of the device. Plasma etching of SiN_x can be performed with high and low bias levels. High bias processes are more anisotropic, but the semiconductor surface is more prone to damage. Low bias etching creates less surface damage, but isotropic etching causes a widening of the trench. A trapezoidal profile of the trench is highly desirable because it can support a void free metal filling and formed integrated field plates can reduce dc-RF dispersion and parasitic capacitance in AlGaN/GaN HEMTs [1,2].

In this work we present a novel process for the formation of slanted gate trenches. The critical etching step is subdivided into 2 steps: (1) a high or low bias plasma etching process to partly form the trench, i.e., the SiN_x layer will not completely etched down to the semiconductor interface, and (2) a wet chemical etch step with phosphoric acid to remove the remaining SiN_x and to generate the desired trapezoidal trench profile. The process sequence is shown in Fig.1. After nitride deposition covering the full wafer and trench lithography, the nitride is etched partially with a plasma etch process to retain the desired residual SiN_x thickness (steps a – c). Then, the resist is stripped (step d) and an isotropic wet chemical etch is applied to thin the nitride layer (step e). The transistor gates will be finalized by a 2^{nd} lithography followed by metal deposition and metal lift-off (steps f). The ratio of the etch depths in the nitride layer generated by plasma and by wet chemical etching will determine the exact geometry of the gate trench. This allows for control of the sidewall angle. Etching, e.g., half of the nitride layer by the plasma process and the remaining half by the isotropic wet process will result in a gate trench with a slanted sidewall of 45° degrees. If already 9/10 of the nitride thickness is removed by plasma etching almost no slant will be obtained after the wet etch. In either case, as the plasma process does not touch the surface, no etch damage will occur.

All experiments were performed on 4 inch Si and n-type SiC wafers with SiN_x films deposited at 345 °C using a Sentech SI500D PECVD tool. The gates were processed in two lithography steps. For the trench layer, ARP 639.10 (PMMA 50k, layer thickness 600 nm) was used as resist. For the (lift-off) metallization layer, a combination of ARP 639.10 (PMMA 50k, 500 nm) and ARP 679.04 (PMMA 950k, 300 nm) was used to generate the desired undercut. Exposure was done on a Vistec SB251 electron beam lithography tool with an acceleration voltage of 50 kV and a dose of 300 µC/cm². A Sentech SI500 ICP tool was used for dry etching of the SiN_x layer by SF_6/He. The wet chemical SiN_x etching was performed with phosphoric acid (85%) at 140 °C; the etch rate was determined on non-structured wafers with interference reflectometry (400 nm … 900 nm) to be 9 nm/min. Size and profile of trench openings in SiN_x were analyzed using scanning electron microscopy (SEM).

A top down SEM micrograph obtained after the combined plasma and wet chemical etching is shown in Fig. 2. Wafer to wafer and wafer within wafer reproducibility tested on 4 GaAs wafers were found to be better than 5 %. From the known nitride thickness and the top and bottom width values, a slanted gate angle of 57 ° is calculated. Fig. 3 shows a SEM cross section of a slanted gate after metallization. Slant and void less metal fill are clearly visible. Initial electrical results were obtained on n-type SiC wafers with an epitaxial layer consisting of 17 nm $Al_{0.25}Ga_{0.75}N$ with a 5 nm GaN cap. Details of the epitaxial structure and processing are presented elsewhere [3]. Fig. 4 and Fig. 5 show the results of dc characterization of small two-finger transistors (2×50 µm). All but the center shot were

functional; the latter was damaged during backside processing. The pinch off voltage (V_{gs}) has a fair distribution and the measured output characteristic is typical for this epitaxy and a length gate of about 250 nm.

We have demonstrated a promising process for the formation of gates. The process combines a partial dry anisotropic plasma with a wet isotropic nitride etch, avoids plasma damage of the semiconductor – metal interface and gives a desired slant. The process will be tested further to explore its full capability.

References

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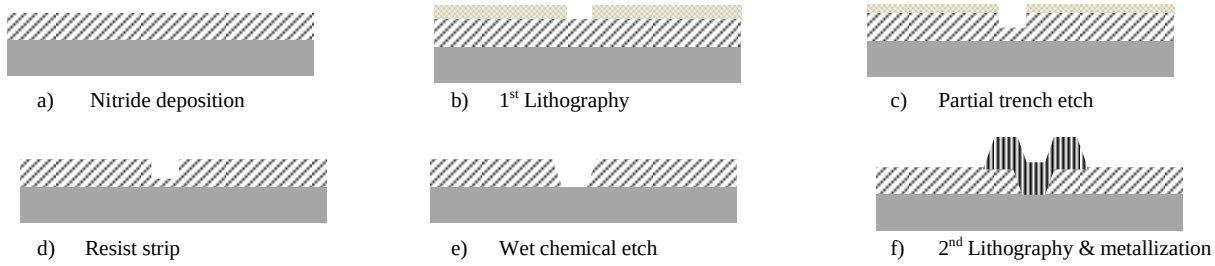

Fig. 1: Schematic process flow for the novel etch sequence

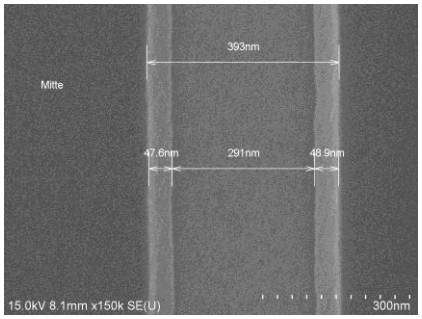

Fig. 2: Top–down SEM view of the slanted trench after dry and wet nitride etch

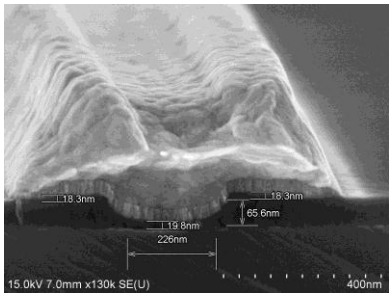

Fig. 3: SEM view of a cross section of a metallized slanted gate on GaAs test wafer. The metal stack is Ti(20nm) /Ir(40 nm)/Au(280nm).

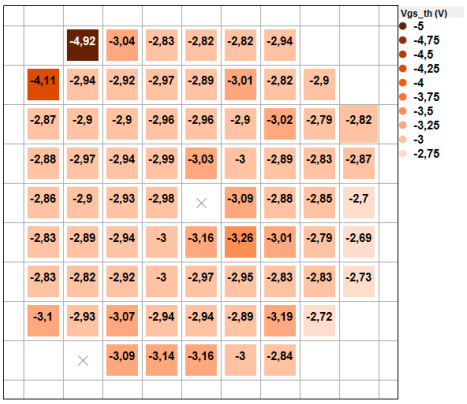

Fig. 4: Pinch-off voltage (V_{gs} in V) across a 4 inch n-type SiC with 17 nm $Al_{0.25}Ga_{0.75}N$ and 5 nm GaN cap.

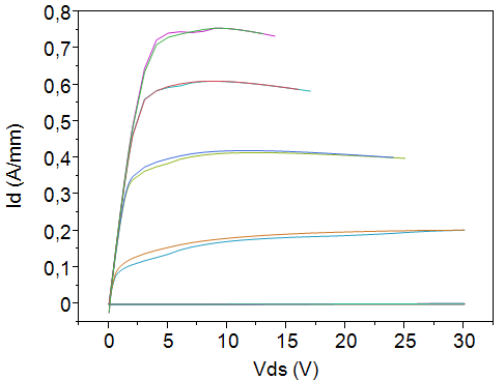

Fig. 5: Typical output characteristics of 2x50 µm devices on n-type SiC. V_{gate} was increased in steps of 1 V from 0V to 5 V