Hetrogenous Integration Schemes of Compound Semiconductors for advanced CMOS and More-than-Moore applications

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The continuation of Moore's law by conventional complementary metal oxide semiconductor (CMOS) scaling is becoming more and more challenging, requireing huge capital investments. On proposed scenario is the implementation of compound semiconductors as parts of advanced CMOS devices for More-than-Moore integration.
The continuation of improved performance characteristics in CMOS manufacturing is coming to a critical point, where electrical properties of silicon introducing a hard stop. One discussed route to increase performance is the hetrogenous integration of compound semiconductors into state of the art CMOS circuits. While growth of III-Vs on silicon shows limited success till now, as well as growing III-Vs in small trench structures shows to be challenging, direct wafer bonding overcomes these challenges.
Wafer bonding is the enabling process technology to make this happen. Two of the key wafer bonding techniques – low temperature fusion bonding as well as temporary bonding and de-bonding are the major subject of this contribution, introducing basic process flows and working principles for their CMOS integration.

Low temperature wafer bonding

The main requirements imposed to wafer bonding by the use of CMOS are: low processing temperature (max. 400°C), no mobile ions and extreme particle cleanliness. Process temperature condition eliminates practically all high temperature wafer bonding processes like standard fusion bonding requiring temperatures between 700°C - 1100°C. The low metal ions traces values acceptable further exclude processes as the robust anodic wafer bonding due to its high level of Na^+ ions contamination. By considering the low contamination criteria the area of CMOS-compatible bonding processes is further reduced.
Fusion bonding is a process based on forming molecular bonds between two surfaces placed into contact which are then further thermally annealed in order to allow the pre-bonds formed at room temperature to transform into strong, irreversible, covalent bonds.
The thermal annealing temperatures required are far too high for CMOS and III-V technology, in which the main temperature limitation is imposed by the Al interconnects or metal interdiffusion (400°C or 450°C for very short time, in the range of minutes).

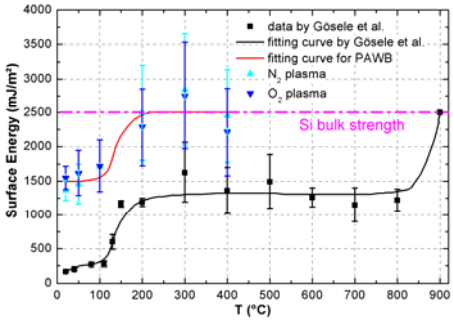

Figure 1. Surface energy of bonded Si/SiO_2 wafer pairs annealed at various temperatures for high temperature oxide bonding and plasma activated wafer bonding using N_2 respectively O_2 plasma. The maximum bond strength of 2.5J/m² is indicated by the dashed-dotted horizontal line. Data for high temperature process was taken from Ref. [1]

Low temperature plasma activated direct wafer bonding is a process that lowers the required annealing temperatures necessary for reaching high bond strength. One example for such an improvement is a pair of native oxide - thermal oxide wafers, where bulk strength can be achieved by plasma activation of wafers prior to bonding with subsequent annealing at 300°C for a short time (0.5 - 1 hour). Figure 1 shows the surface energy (bond strength) characteristics as a function of the annealing temperature for Si/SiO_2 wafer pairs with and without plasma activation prior to fusion bonding. The attempt to explain the newly obtained results using the known model for silicon hydrophilic bonding failed.
Comparison with the high temperature process shows that high bond strength values correspond to a state where all water is removed from the bonding interface. At this stage the bond strength is limited by the limited contact area due to the roughness of the surfaces. Starting from 200°C the nanogaps at the bonding interface are closed, so the surfaces are in full contact and bulk strength is reached [2].
In order to clarify the gap closing mechanism plasma activated wafer surfaces were investigated using surface sensitive techniques like atomic force microscopy, spectroscopic ellipsometry and Auger electron analysis.
Based on this research a theoretical model was developed, which explains the specific results of this process and allows better process control.

This model is based on the classical process model, but proposes a different mechanism for gap closure at low annealing temperatures. The model for plasma activated wafer bonding will be presented in detail.

Temporary Bonding

Thin wafer processing is a critical technology for through wafer via manufacturing heterogeneous integration of compound semiconductors. Thin wafer processing allows to reduce the aspect ratio of the vias, thereby reducing the total processing cost and enables ultra-thin packages for handheld applications.

Temporary bonding to a rigid support carrier and debonding after backside processing have been used for thin wafer handling/processing for many years. However, so far all the debonding methods imposed severe limitations on the manufacturability. For light induced debonding the carrier had to be transparent and for solvent based debonding the carrier had to be perforated. For thermally induced debonding ("slide-off debonding") the debonding temperature had to be below the reflow temperature of the solder bumps, which limited the maximal process temperature of the adhesive. In the past the debonding method, the adhesive properties and the carrier properties were closely linked to each other. This link between debonding method, adhesive and carrier imposed severe limitations on the manufacturability [3].

In a nutshell the industry demands standardized processes for thin wafer handling. The revolutionary ZoneBOND® technology achieves just that – standardized and material independent processes and equipment. With ZoneBOND® technology the debonding process is not at all a function of the adhesive any more – debonding has become a function of the carrier. The ZoneBOND® carrier has two zones, which differentiate by the degree of adhesion between the adhesive and the carrier. The adhesion in the center zone is reduced, whereas full adhesion is at work in the edge zone. Figure 2 shows a schematic drawing of a temporarily bonded device wafer to carrier by applying the ZoneBOND® process. It is important to note that the surface of the device wafer does not have to be treated at all for ZoneBOND® which makes the technology compatible with any kind of surface passivation. This is especially important with regards to assembly after thin wafer processing. Debonding methods which rely on surface modifications of the device wafer have the inherent risk of causing adhesion problems

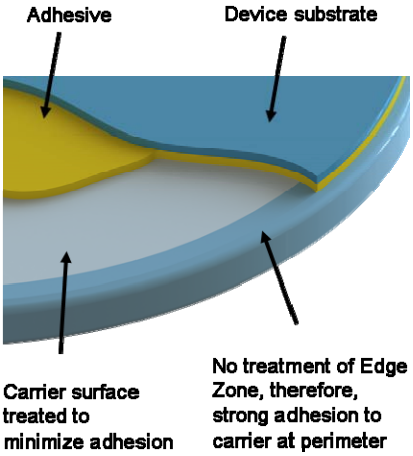

Figure 2. ZoneBOND® carrier schematic

Acknoledgments

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References

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[2] V. Dragoi, F. Kurz, T. Wagenleitner, C. Flötgen and G. Mittendorfer, *Wafer bonding for CMOS Integration and Packaging, in press*

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