Improved Near Junction Thermal Transport Using GaN on Diamond

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Keywords: GaN on Diamond, Diamond, GaN

Abstract

This paper discusses the ongoing results of Raytheon's work on the Near Junction Thermal Transport (NJTT) effort of the Thermal Management Technologies (TMT) program under contract with DARPA. The goal of this work is to increase the power handling capability of today's state of the art GaN by 3X. Our approach and results are discussed in this paper.

INTRODUCTION

As GaN device technology matures into production it has become clear that thermal impediments are limiting GaN from achieving its full potential. One heat management strategy is to replace the substrate the GaN epi is grown on with a much higher conductivity diamond substrate. Here we describe the results of a program funded by DARPA to increase the power handling capability of today's start of the art GaN by 3X. The approach at Raytheon is to manufacture devices on GaN on Diamond substrates that have parallel gates whose spacing is reduced by a factor of three.

GaN on Diamond wafers were supplied to Raytheon by Group4 Labs, an industry leader in GaN on Diamond wafer development. To make the GaN on Diamond wafers, GaN was lifted from industry available wafers and bonded to a diamond wafer using Group4 Labs' patented transfer process [1] (Figure 1).

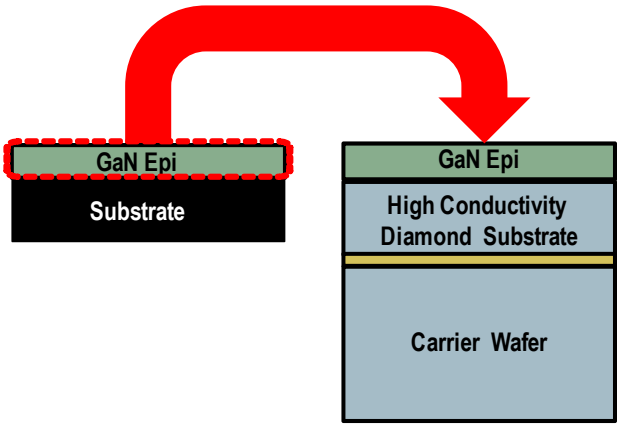

Figure 1. GaN epitaxial material is transferred from its growth substrate to a diamond substrate.

TEST VEHICLE AND PROCESSING

To demonstrate a 3X improvement in power density we developed a test vehicle that output the same power in 1/3 the space. GaN transistors for power applications have multiple gates placed in parallel, and the spacing between fingers is determined by lithography restrictions as well as thermal considerations. For the test vehicle we chose a standard GaN transistor with 10 fingers, each with 125um of gate width, with 40um of spacing between each finger. Thermal analysis of this FET at typical power dissipations of an X-Band power amplifier places channel temperature at 80°C above baseplate temperature. If gate to gate spacing is reduced by 3X and placed on a diamond substrate, analysis shows that channel temperatures will actually be cooler. Hence our test vehicles for the program were two 10x125um transistors with 40um and 13um gate to gate spacings, as shown in Figure 2. With decreased channel temperatures, FETs on diamond can now have gate fingers spaced closer together, increasing power handling density with the potential to shrink overall MMIC size and reduce total cost

The GaN on diamond wafers were mounted on a thermal expansion-matched thick carrier plate for robust wafer handling and reduction of wafer bow and were then processed in Raytheon's foundry, located in Andover, MA. The wafers were processed using stepper photolithography with HEMT gates formed using e-beam lithography.

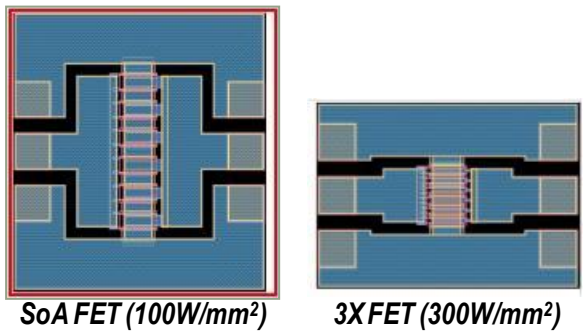

Figure 2. Test Vehicle Structure showing 3X Power handling improvement.

ELECTRICAL AND THERMAL TEST DATA

To evaluate the impact of diamond substrates, DC, RF, and thermal measurements are taken on identical devices on both diamond and baseline substrates. DC characterization includes pulsed IV curves that examine the quality of the epi by analysis of trapping, knee voltage, and Imax. RF characterization is accomplished by using both small-signal and large-signal transistor performance. Small-signal measurements compare gain and f_{max}. Large-signal measurements are taken on a Maury loadpull system where individual HEMTs are optimized for Power and PAE under identical bias and hot plate temperature conditions. By comparing peak Power and PAE, we ascertain how different thermal properties of substrates impact RF performance of HEMTs.

Thermal characterization is performed at Raytheon by using DC bias to dissipate a known amount of power in a HEMT and then measuring the resulting average device temperature.

Characterization of diamond properties and the thermal stack of the devices is performed at Stanford using the Time Domain Thermoreflectance (TDTR) technique. This technique enables extraction of component thermal resistances in the GaN on Diamond stack, providing an improved understanding of how individual layer properties drive overall device thermal performance

Georgia Tech performs micro Raman measurements on both baseline GaN and GaN on Diamond devices. These measurements enable the mapping of temperature and stress in the GaN buffer layer near the active regions of the device under DC bias conditions. This provides local resolution of channel temperatures.

ACKNOWLEDGEMENTS

This material is based upon work supported by DARPA under Contract No. W31P4Q-11-C-034. Any opinions, findings and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of DARPA.

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REFERENCES

[1] Babic, Dubrakvo *et al.* "GaN on diamond Field Effect Transistors: From Wafers to Amplifier Modules," MIPRO/MEET International Conference, May 2010

ACRONYMS

GaN: Gallium Nitride
PAE: Power Added Efficiency
MMIC: Monolithic Microwave Integrated Circuit