## SiN/Ge Lift-off: A Method for Patterning Films Deposited at High Temperature

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## **Abstract:**

Lift-off processing is a ubiquitous microfabrication technique that typically uses one or more patterned layers of photoresist to selectively place a thin film of metal (or dielectric [1]) on a sample surface. While photoresist-based lift-off has been a work-horse of the semiconductor industry for decades, it does have one key disadvantage that limits the versatility of the technique: conventional photoresists reflow at relatively low temperatures, typically between 100 - 150 °C. Since most dielectrics and semiconductors require deposition/growth temperatures greater than 300 °C to achieve high electrical and/or structural quality, photoresist is not a viable option for patterned lift-off of these materials.

To circumvent the low temperature limitations of conventional lift-off, we have developed a novel inorganic lift-off technique that uses silicon nitride (SiN) and Ge to form a bi-layer structure for patterning. The process flow starts by depositing a uniform layer of Ge that is at least 1.6 times the thickness of the film to be lifted off. Next, SiN is blanket deposited over the Ge to a thickness of at least 50 nm. Conventional lithography processing is then used to pattern resist, as shown in Fig. 1, allowing access to the SiN. By using a fluorine-containing dry etch such as an inductively-coupled SF<sub>6</sub> plasma, windows in the SiN can be etched anisotropically to access the Ge layer, while the same plasma conditions isotropically etch the Ge, creating an undercut as illustrated in Fig. 2. Following photoresist stripping, Fig. 3 shows that the patterned bi-layer of SiN/Ge now serves as a mask for selective placement of films that can be deposited at temperatures much higher than 150 °C. While the melting point of Ge is 938 °C, the upper temperature limit of this technique depends on the specific substrate used, and whether it is thermodynamically stable with Ge.

As a proof-of-concept demonstration, Fig. 4 and Fig. 5 show application of this method before and after, respectively, lift-off of evaporated Ti/Au (20/80 nm). To remove the SiN/Ge mask and excess Ti/Au, the sample was immersed in heated hydrogen peroxide  $(H_2O_2)$ , which readily etches Ge. Since this initial demonstration, we have found that  $XeF_2$  gas can also be used as an alternative to  $H_2O_2$ , enabling a dry lift-off process. We are presently investigating the application of this technique to selectively regrow epilayers (for reduced contact resistance to GaN transistors) with molecular-beam epitaxy (MBE). Fig. 6 shows the robust integrity of SiN overhangs, which are subjected to MBE GaN regrowth at 670 °C. An overview of this technique, along with the most recent examples of application will be presented in our talk.

## **References:**

[1] D. J. Meyer, R. Bass, D. S. Katzer, D. A. Deen, S. C. Binari, K. M. Daniels, and C. R. Eddy Jr, "Self-aligned ALD AlO<sub>x</sub> T-gate insulator for gate leakage current suppression in SiN<sub>x</sub>-passivated AlGaN/GaN HEMTs," *Solid-State Electronics*, vol. 54, pp. 1098-1104, 2010.

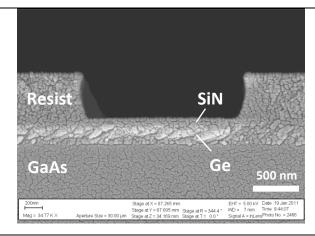


Fig. 1: SEM cross-section of evaporated Ge (200 nm) and PECVD SiN (50 nm) film layers on a GaAs substrate. S1805 resist was patterned using conventional lithography.

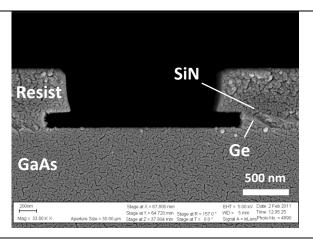


Fig. 2: SEM profile of feature after SF<sub>6</sub> ICP plasma etching to open SiN and undercut Ge.

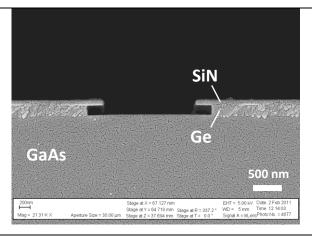


Fig. 3: SiN/Ge bi-layer profile after removal of resist with acetone.

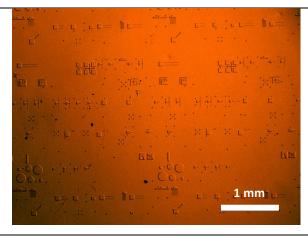


Fig. 4: Plan-view micrograph of SiN/Ge patterned sample after evaporation of Ti/Au (20/80 nm).

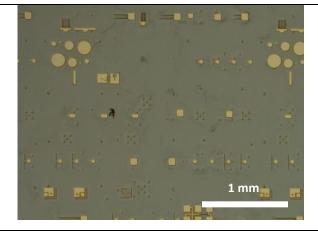


Fig. 5: Plan-view micrograph of Ti/Au patterned features after SiN/Ge lift-off in heated H<sub>2</sub>O<sub>2</sub>.

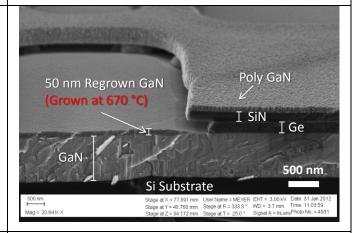


Fig. 6: SEM cross-section of SiN/Ge feature after MBE growth of 50 nm n<sup>+</sup> GaN performed at 670 °C.