Multi-Guide Vertical Integration in InP – A Regrowth-Free PIC Technology for Optical Communications

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Abstract

This paper describes the fundamentals and applications of the multi-guide vertical integration platform in InP, an authentic cost-efficient photonic integrated circuit technology for optical communications.

INTRODUCTION

Monolithic photonic integrated circuits (PICs) provide an automated (optical alignment by means of lithography), robust (no moving parts), small footprint (no bulk-optics assemblies) and volume-scalable (wafer start rather than optical sub-assembly scaled) component solution to fiber-optics communication systems. InP-based materials are and will continue to be the base materials for the transmitter, receiver and transceiver components in such systems, since they are the direct bandgap semiconductors perfectly suited for emission and detection in the most important wavelength ranges around 1.3μm and 1.5μm. At the same time, InP and related compound semiconductors offer a variety of choices for optical guiding and guided wave management. Together, an ability to emit / detect in the required wavelength ranges and an availability of the highly functional waveguide circuitry in this range make the InP-based compound semiconductors a natural material choice for the optical communications PICs. Indeed, such PICs have been researched over the last thirty years and, eventually, are becoming an industry accepted technology [1]. Still, their market penetration is not significant, while new applications are emerging, e.g. coherent transmission and optical interconnects, which are poised to create sizable markets provided there are high-performance and low-cost PICs to support them. A versatile and cost-efficient photonic integration platform in InP is the key to this problem and the multi-guide vertical integration (MGVI) is one such platform, developed and commercialized by OneChip Photonics Inc. It is implementable in one-step epitaxial growth process, which not only eliminates yield issues associated with the multiple growth steps, but also allows for decoupling of epitaxial growth and wafer fabrication. This, in turn, enables for outsourcing each of them to commercial InP foundries (at this time mostly RF electronics, not photonics, foundries) and practically implement a fabless model for PICs. This paper explains the basics of MGVI platform, describes its key building blocks, and reports on exemplary PICs for optical communications in two most massive and cost-sensitive segments of the market: fiber-to-the-home (FTTH) and fiber-optics interconnects (FOI).

MULTI-GUIDE VERTICAL INTEGRATION PLATFORM

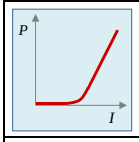
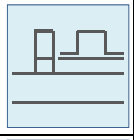
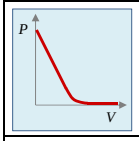
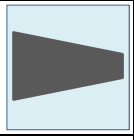
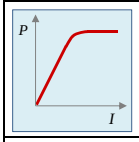
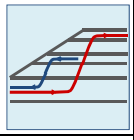
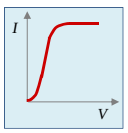
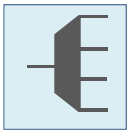
The key to the photonic integration in InP is an ability to combine different waveguide devices (and materials they are made from) for different – active and passive – functions onto one InP substrate. In a case of the optical communications PICs, the circuit functionality includes, but not limited to: light emission, modulation, amplification and detection, in addition to waveguiding, guided wave routing and space or wavelength division (de)multiplexing. These functions require different semiconductor materials: waveguide detector typically has its core layer bandgap wavelength λ_G well above, emitter and amplifier – close to, and passive devices – well below the operating wavelength λ. Also, they need different doping and waveguide designs: the active waveguides are doped as a vertical PIN structure and usually are highly confining waveguides, while the passive waveguides are preferably not doped at all and often require to be diluted. It is clear that such features cannot be combined in a simple planar waveguide structure with one – common – waveguide, but rather need different waveguides made from different materials. There are two distinct approaches to this problem: different semiconductor materials either are locally grown, e.g. by etch-and-regrowth or selective area growth process, thereby enabling for a planar waveguide structure with butt-coupling between the functional waveguides, or they are vertically stacked in one growth step process, forming a multi-guide vertical waveguide structure with an evanescent-field coupling between the functional waveguides. The MGVI is based on a consistent implementation of the second approach and extends it from a simple twin-guide structure [2] to sophisticated multi-functional PICs [3], in which the functional waveguides are vertically stacked in an ascending order of their λ_G, while adiabatic transitions between them are affected by lateral tapers defined at each guiding level [4]. Then, the functional waveguide at each vertical level can be designed and optimized independently. MGVI allows for a large variety of materials, doping levels and waveguide

configurations, but on expense of sophisticated design (both the epitaxial structure and device layout), by shifting manufacturing challenges from multiple-step epitaxy to many-layer epitaxial growth (in certain cases 90+ layers) and multiple etch step fabrication process (number of consecutive etches depends on the PIC functionality and may reach 6-7 steps). Both the many-layer epitaxial growth and multiple etch step wafer fabrication are commercially available, by means of the MOCVD growth and the optical stepper lithography, respectively, and can be used for outsourcing the PIC manufacturing. This is exactly what OneChip Photonics does under its fabless model: all the examples in the following Sections represent the devices commercially MOCVD grown on 4" semi-insulated Fe:InP substrates and processed in the commercial foundry by using I-line optical stepper at each lithography step. The regrowth-free process also includes standard, yet adjusted to the MGVI needs, dry and wet etching, passivation, planarization and metallization steps.

Design And Fabrication Building Blocks

In addition to decoupling of the epitaxial growth and wafer processing, decoupling of the device and circuit designs is the key to the fabless PIC manufacturing. In the MGVI platform, it is achieved by using a building block approach, in which a limited number of the pre-verified devices form a library of generic functional elements and photonic circuit is designed based on these elements.

TABLE I
KEY BUILDING BLOCKS OF MGVI PLATFORM

Active Waveguide Devices		Passive Waveguide Devices	
	**DFB Laser** Used as an on-chip source in all Tx and TxRx PICs, with an adjustment for wavelength and speed.		**Ridge Waveguides** Etched ridge waveguides and various elements of waveguide circuitry, used in all MGVI PICs.
	**EA Modulator** Operates on electro-absorption under the quantum-confined Stark effect and used in all Tx-EML PICs.		**Spot-Size Converter** Used for a (very) low insertion loss, high displacement tolerance fiber coupling – in all MGVI PICs.
	**SO Amplifier** Designed as an on-chip optical pre-amplifier to the PIN-WPD and used only if ASE is filtered out.		**Wavelength Splitter** A (very) coarse WDM based on the dispersion properties of vertically stacked tapered waveguides.
	**Waveguide PD** Used as an on-chip detector in all Rx and TxRx PICs, with an adjustment for wavelength range / speed.		**Planar WDM** Diffractive echelle grating and arrayed waveguide grating based in-plane dense or course WDM.

On the active device side, the key building blocks are: a distributed feedback (DFB) laser, an electro-absorption modulator (EAM), a semiconductor optical amplifier (SOA) and a waveguide photodetector (WPD). On the passive device side, the MGVI building block library includes shallow / deep and strong / diluted ridge waveguides, as well as low insertion loss junctions between them, mode / spot-size converters (SSC), a directional coupler, a beam splitter, and a vertical / planar wavelength-division multiplexers (WDM). Some of the key MGVI building blocks are summarized in Table I, with details of the design, fabrication and characterization reported elsewhere [3, 5-12].

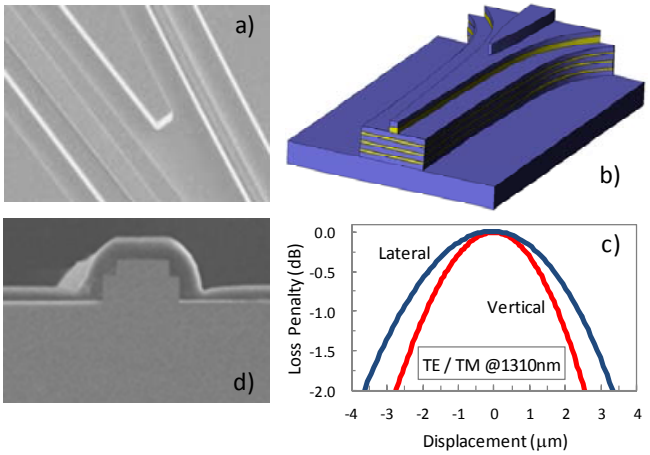


Figure 1. On-chip SSC – the most generic MGVI building block. a) and d) – the top view and vertical cross-section SEM images, respectively; b) – sketch of the SSC featuring multiple-step lateral tapering; c) – measured insertion loss penalty vs. displacement from the optimal alignment position.

An example of the MGVI generic building block is an on-chip SSC for a low insertion loss and high displacement tolerance coupling to a cleaved single-mode fiber. In fact, it is the most generic of all MGVI building blocks since it is used in each and every MGVI PIC. The schematic layout, SEM images and key characteristic of the device – insertion loss penalty as a function of the displacement from the optimal alignment position – are presented in Fig. 1. While the fiber to SSC mode overlap is only 0.4dB, the displacement tolerance at 1-dB penalty exceeds ±2.5μm in both lateral and vertical directions, thereby enabling for a highly efficient and well controlled passive alignment by using commercial pick-and-place machines. Given that this is the only required alignment – all other optical alignments done by means of the stepper lithography – the SSC reduces the optical assembly to just one passive alignment step.

Different yet compatible combinations of the building blocks allow for a wide range of the MGVI PICs featuring functional (e.g. emit *and* detect or demultiplex *and* detect) / and parallel (e.g. detect in the wavelength demultiplexed channels) integration, examples of which are provided in the following sections. At the same time, by limiting the building block library to a relatively few generic functional elements, new PIC development is reduced to the circuit design and fabrication, leaving the underlying device physics and processing behind. This greatly simplifies new product introduction and shortens design re-spin cycles.

TRANSCEIVER PICS FOR FTTH

Continuing growth of the fiber to the home (FTTH) deployment has created the most massive and cost-sensitive telecom market to date. The key FTTH component is the optical network unit (ONU) transceiver, which transmits in 1310nm / receives in 1490nm, while multiplexing these two wavelengths sharing the same fiber. The bidirectional transceiver PIC that provides these functions is an example of the functional integration and shown at the top of Fig. 2. A 4-guide MGVI structure comprises, top to bottom, a WPD for detection in 1490nm range; a DFB laser for emission at 1310nm (complemented with a power monitor formed at the same guiding level); a passive waveguide used for on-chip routing and connection to a common optical port; and a diluted fiber-coupling waveguide forming a SSC for a low insertion loss, high displacement tolerance coupling to / from the PIC. The 0.4mm x 2.8mm InP chip provides all the optical functionality required for ONU transceiver.

Light-current and spectral characteristics of the on-chip laser, as well as its eye diagram, are shown in the bottom part of Fig. 2. It is seen that even though laser's efficiency drops with the temperature, mainly because of self-heating in N-up / side P-contact configuration chosen for the reasons of MGVI compatibility [8], still the power that this on-chip source emits is quite significant and certainly sufficient for the target application. Besides, a better thermal management in the PIC package is feasible, which can further improve the laser efficiency at elevated temperatures. As it concerns to the spectral properties of the laser, MGVI-compatible DFB

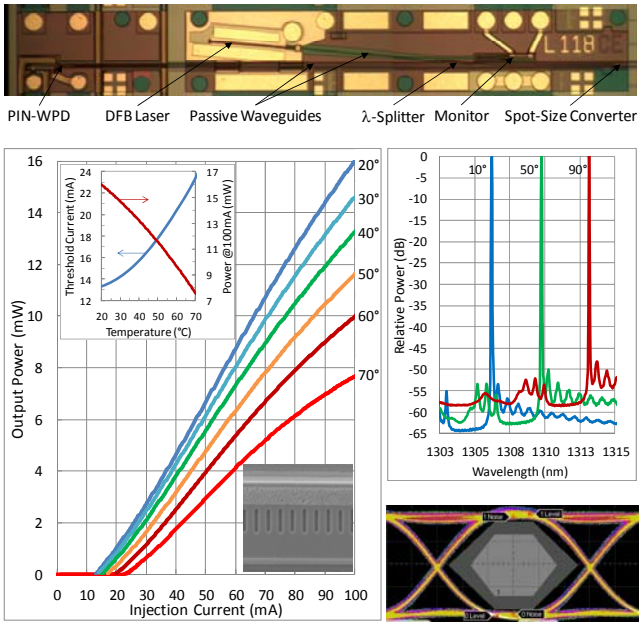


Figure 2. Full optical duplex PIC for ONU transceiver applications in FTTH networks. Top – optical microscope image of a 0.4mm x 2.8mm die after singulation; bottom – key performance features of the on-chip DFB laser. Shown in the bottom right corner of the light-current characteristic is the SEM image of the laser's vertically-coupled surface-etched grating.

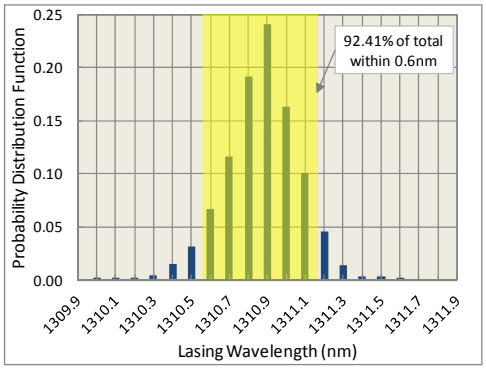


Figure 3. Probability distribution for lasing wavelength of on-chip DFBL in FTTH PICs designed for operation at 1310nm. Total of 6,460 devices tested at 25C. Median wavelength: 1310.9nm, standard deviation: 0.2nm.

laser design and, more specifically, the use of the 3rd order surface-etched grating actually provides certain advantages [13]. First, complex coupling without etching through the gain region, enabled by such a grating, improves the mode stability while also increasing the side-mode suppression ratio (which typically is in 50dB+ range, as it is seen from Fig. 2). Second, a relatively low optical confinement of the lasing mode with the active region (roughly half of that in the best commercial discrete devices), pre-determined by the requirement for coupling with the surface-etched grating above and the passive waveguide below the laser guide, also means low manufacturing variability of the Bragg wavelength, which, in a combination with the grating defined by the stepper lithography and limited to InP layers not subjected to the growth variability, results in an exceptional reproducibility of the laser wavelength. To illustrate this, Fig. 3 shows probability distribution for the on-chip DFB laser wavelength over 4" wafer filled with the devices similar to that shown in Fig. 2. It has a standard deviation of only 0.2nm – significantly lower than that for conventional stand-alone lasers, which is an intrinsic property of the MGVI laser design and extends to all the PICs featuring this building block.

RECEIVER AND TRANSMITTER PICS FOR FOI

Fiber-optics interconnects (FOI), emerging as the only practical solution to the high-capacity point-to-point connectivity in new generation data centers, warehouse-scale computers and likes, provide another example of the massive, cost-sensitive market well served by the MGVI technology. The enabling components are the ultra-compact, power-efficient and low-cost optical transmitters and receivers with an aggregate bandwidth of 100+Gb/s and capability for a transmission in a single-mode fiber over reach distance up to 2km. Several 100Gb/s FOI architectures are being discussed now, of which the most promising – and the most accepted by industry – are the 4x25Gb/s point-to-point links operating in 1.3μm spectral range at 25Gb/s signaling speed and quadrupled by space or LAN wavelength or course wavelength division multiplexing

(SDM or LWDM or CWDM, respectively). The MGVI platform allows for an integrated solution to the transmitter and the receiver optics in each of them. Furthermore, either the transmitter or the receiver PICs for SDM, LWDM and CWDM interfaces can be co-located and co-processed on one transmitter or receiver wafer, respectively, since they all are based on the same building blocks. A combination of the multi-project wafer and the building block approaches allows for the further improvement of the cost efficiency.

As an illustration of the MGVI technology capabilities in the 100Gb/s FOI area, shown in the Fig. 4 are the 4x25Gb/s CWDM receiver PIC and some of its key characteristics. This is an example of the functional (demultiplex *and* detect) *and* parallel (detect in 4 wavelength channels) integration based on the MGVI platform. A 3-guide MGVI structure comprises, top to bottom: an active waveguide bearing the PIN-WPD for detection in each of 4 CWDM wavelength lanes; a passive waveguide for demultiplexing the optical signals in these lanes and also routing them to / from the planar waveguide demaltiplexer; and a diluted waveguide forming a SSC for a fiber coupling. Fig. 4 a) presents the optical microscope image of as fabricated receiver PIC featuring the diffractive echelle grating (DEG) based 1x4 demultiplexer and 4x25Gb/s PIN-WPDs inserted in its output waveguides. The die size is only 0.45mm x 2.2mm, the smallest ever reported for a 100Gb/s receiver optics. Fig 4 c) shows typical frequency response of the PIN-WPD, with the 3-dB bandwidth of about 20GHz. Shown in Fig. 4 b) is the SEM image of the etched DEG – the key element of

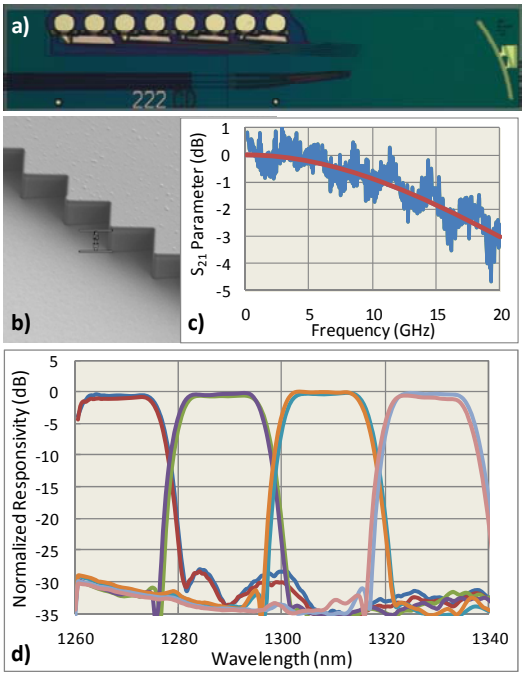


Figure 4. 4x25G CWDM receiver PIC for 100Gb/s FOI. a) – the optical microscope image of as-fabricated chip after die singulation; b) – the SEM image of the etched DEG; c) – the frequency response of the PIN-WPD; d) – normalized fiber-coupled responsivity spectra in TE / TM polarizations.

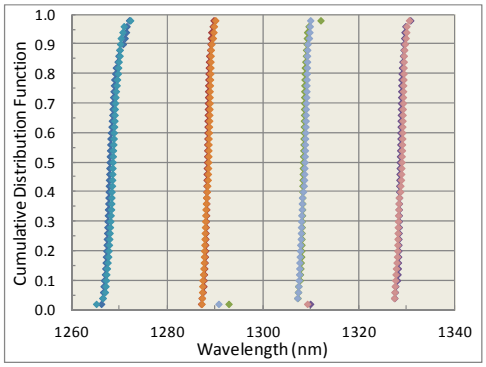


Figure 5. Cumulative distribution functions for the centre wavelengths of the DEG-based 4-channel CWDM filter at 25C. Total of 265 integrated receiver chips from different wafers / lots tested in both TE and TM polarizations. Average inter-channel spacing is 20.08nm (target: 20nm).

the on-chip demultiplexer. Quality of the DEG etch affects the passband spectra shown in Fig 4 d), which have a ripple-free 15-nm wide (at 1-dB down) flat-top passband and a crosstalk approaching -30dB – amongst the best CWDM filters ever made in any semiconductor material. The fabrication process is quite reproducible, too. Fig. 5 presents the cumulative distribution functions for the center wavelength in each of 4 CWDM lanes of the receiver PIC shown in Fig. 4a), resulted from testing of a large number of the devices. It is seen that not only the center wavelengths are on target, but also tightly distributed.

Conclusion

The MGVI in InP is the versatile PIC technology that allows for the cost-efficient and volume-scalable photonic component manufacturing by decoupling the epitaxial growth and wafer processing while outsourcing both to the pure-play commercial foundries. Yet it delivers the state of the art transceiver, transmitter and receiver PICs for optical communications. Techno-economical advantages offered by the MGVI technology uniquely position it as an attractive option for the cost-sensitive and performance-challenging component markets, like the FTTH and FOI markets.

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References

[1] F. Kish, *et al – IEEE J. STQE*, **17**, 1470 (2011).
[2] Y. Suematsu, *et al – IEEE J. Quantum Electron.*, **11**, 457 (1975).
[3] V. Tolstikhin – *Proc. IPRM'11, Paper 6.2.1* (2011).
[4] V. Tolstikhin, *et al.* – US Patent No. 7,532,784 (2009).
[5] V. Tolstikhin, *et al.* – *IEEE Photon. Technol. Lett*, **21**, 621 (2009).
[6] V. Tolstikhin, *et al – Proc. IPRM'09, Paper TuB1.6* (2009).
[7] S. Kuntze, *et al. – Proc. IPR'2010*, Paper ITuC (2010).
[8] V. Tolstikhin – *Proc. IEEE IPC*, Paper WX2 (2010).
[9] Y. Logvin, *et al – Proc. IP'2011* (2011).
[10] F. Wu, *et al – Proc. IPR' 2011*, Paper ITuC3 (2011).
[11] C. Watson, *et al – Proc. IEEE IPC*, Paper TuQ3 (2011).
[12] Y. Logvin, *et al – Proc. IEEE IPC*, Paper ThZ2 (2012).
[13] K. Pimenov, *et al. – Proc. NUSOD'2010*, Paper TuC3 (2010).