SESSION 4a:
PROCESS – BACKSIDE
Chair: Michelle Bourke, *Oxford Instruments Plasma Technology*

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The backside processing session this year considers the formation of vias in SiC, GaAs and InP. The session begins with a joint paper from SPTS Technologies and WIN Semiconductors. This paper will focus on the development of an 85µm diameter, 100µm deep SiC backside via etch process on 100mm SiC/GaN wafers bonded to carriers. The results will show SiC etch rates >1.3µm/min. The second paper in this session is a joint paper from TriQuint Semiconductor (Texas) and Brewer Science. This paper will discuss the development of a mounting process that enables the thinning of the substrate to the required thickness for such devices is presented with consideration to critical process requirements including total thickness variation (TTV), grind thickness uniformity, damage removal, etch resistance, and electrical parameters. Following on from a backside process relating to GaAs, the third paper in this session is from NTT Photonics Laboratories, NTT Corporation. This paper will discuss a backside process for thinning 3-inch InP substrates down to 50µm, forming dense vias with good uniformity across the whole substrate, and backside-metal patterning, which is applicable for up to Y-band SMMICs. The final paper is this session is a joint paper from the Department of Electrical Engineering, University of Notre Dame and MicroLink Devices. This paper will compare several process alternatives for forming small-area, high-density vias in Indium-bearing III-V materials by dry etching. Three different chemistries will be considered, Cl_2/Ar, $BCl_3/Cl_2/Ar$, and $SiCl_4/Ar$.