Advances in Back-side Via Etching of SiC for GaN Device Applications

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Abstract

This paper will focus on the development of an 85µm diameter, 100µm deep SiC back-side via etch process for production. 100mm SiC/GaN wafers bonded to carriers were provided by WIN Semiconductors Corporation and etched at SPTS using an APS process module. Etch rates >1.3µm/min with cross-wafer uniformities of <±5% have been achieved along with selectivities to a patterned Ni hard mask in the range 30-40:1. A unique descum process has been introduced that reduces the defect level from up to 100% to <1%. Selectivities of >30:1 between the SiC and the GaN material have been obtained. Etch by-products are shown to be readily removed for compatibility with metallisation. Data is included on the etching of the GaN layer within the same process module. GaN etching is shown to be selective to the underlying Au metal and is compatible with end-point detection. Via resistances <6E-3Ω have been achieved.

INTRODUCTION

The high breakdown voltage and high electron mobility of GaN make it an attractive material for high power device applications [1]. GaN is typically grown on SiC substrate wafers. Therefore the implementation of back-side vias involves the deep etching of SiC to form conducting pathways to the front-side circuitry [2,3].

Compared to GaAs the material properties of SiC and GaN make them much more challenging to plasma etch. Energetic plasma processes are required to deliver productive SiC etch rates whilst maintaining high enough selectivity to the masking layer and low enough wafer temperature to preserve the bonding and prevent de-lamination. This requires metal masks and careful attention to the method of wafer clamping and temperature control. Due to the ground finish of the pre-etched SiC surface descum break-through steps are essential in minimising defects within the vias to maximise device yields. In such an energetic plasma environment it is challenging to maintain smooth enough SiC walls for subsequent seed metal deposition/electro-plating and to preserve selectivity to the GaN. The build up of relatively low volatility etch by-products within the via and upon the surfaces of the plasma reactor requires effective wet cleans to be developed for both the wafer and the reactor.

EXPERIMENTAL

Substrates for etching were prepared by WIN Semiconductors. The 100mm diameter GaN/SiC wafers were temporarily bonded face down to a 100mm carrier. After SiC grinding to ~100µm thickness an electro-plated Ni mask was patterned ready for the SiC via etch. Following via etching the wafers were wet cleaned to strip the mask and clean the via of polymer. The GaN layer was then etched, using the SiC via as the mask, stopping on the front-side Au metal. All etching was carried out in an SPTS APS process module. A schematic of the module is shown in Figure 1.

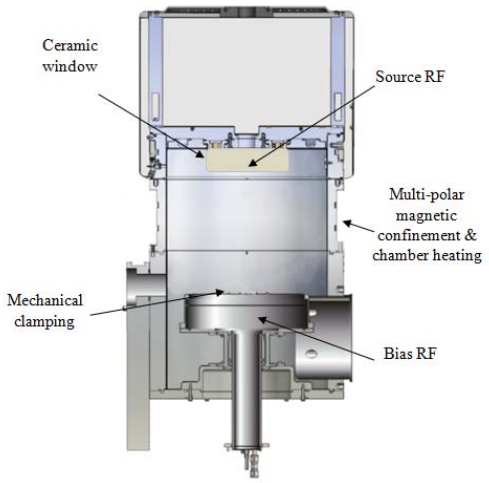

Figure 1 Schematic diagram of the APS plasma etch module.

The reactor is designed with a doughnut-shaped source RF coupling ceramic (13.56MHz at up to 2.2kW), and a heated chamber (set to 50-60°C) with multi-polar magnetic confinement. This arrangement delivers plasma densities in the range 10^{12}-10^{13}cm^{-3}, typically 10x higher than conventional ICPs. The etch processes used SF_6/O_2/He and Cl_2/BCl_3 chemistries for the SiC and GaN, respectively. A propietary descum process was developed as part of the SiC via etch in order to reduce/eliminate the formation of pillar defects. Mechanical clamping was used to ensure reliable temperature control during the SiC and GaN etch steps. The platen temperature was set to 10°C. Optical emission spectroscopy (OES) was used to end-point the GaN etch. Wet chemical via cleaning was also investigated. Processed wafers were analysed using optical microscopy, cross-sectional SEM, profilometry and temperature label measurement.

RESULTS

Wafer temperature was assessed using '4 level micro-strips' (RS Components). These temperature stickers record the peak temperature. Table I summarises the peak temperatures for various wafer types for a 5 minute etch time when the platen is set to 10°C. These temperatures are safely below the the maximum allowable (dictated by the temporary bonding layer) which is 130°C in this case.

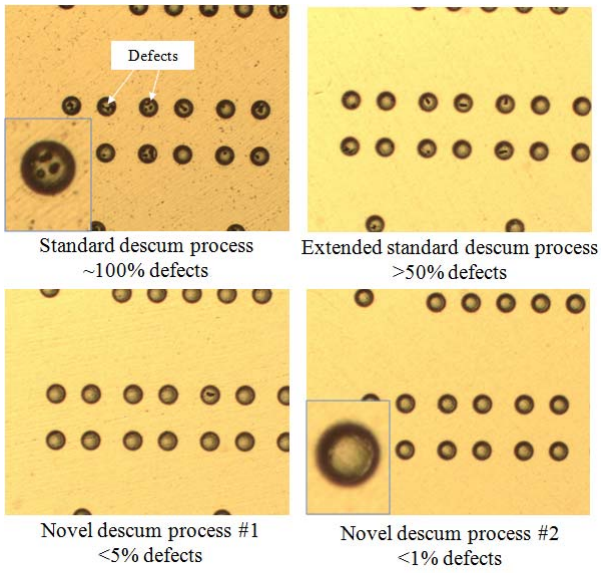

Figure 2 Optical images showing the effect of descum conditions on pillar defect density.

Due to the wet chemical etches of the metal seed layers and the SiC grinding that take place prior to the SiC via etch it is necessary to introduce a descum step as part of the via etch process. Optical images of SiC vias are shown in Figure 2 after partial etching with a range of descum conditions. Standard descums are ineffective, resulting in defectivity levels of 50-100%. A proprietary approach has been developed that substantially reduces pillar defectivity to <1%.

TABLE I
WAFER TEMPERATURES FOR SILICON CARBIDE VIA ETCHING

Wafer type	Wafer temperature (°C)
Sapphire carrier	100
Bulk SiC	80
SiC bonded to carrier	116

Figure 3 shows the SiC etch rate and the Ni mask selectivity for the main etch conditions as a function of bias power. The wafers were run with the optimized descum but the impact of the descum on the etch rate and selectivity has been subtracted.

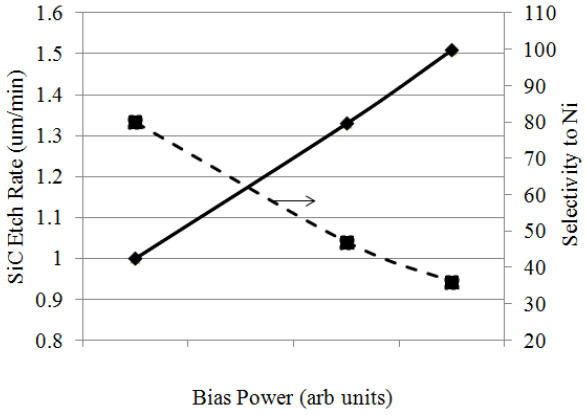

Figure 3 SiC via etch rate and mask selectivity vs bias power. SF_6/O_2/He flow rate ratio 10:1:7.

The data clearly shows that there is a balance required between maximizing the etch rate and conserving sufficient Ni mask by optimizing the selectivity.

Figure 4 shows selectivity to the GaN underlayer across a similar bias power range. The improvement in selectivity with reducing bias power makes a 2 step (soft landing) approach appropriate for this application.

Having investigated the etch rate and selectivity trends it was necessary to focus on improvements to the sidewall roughness of the via. Figure 5 shows the impact of chemical dilution on the SiC etch rate and mask selectivity. Here the He flow was increased so as to be the primary process gas. There is a corresponding reduction in the slopes of the graphs. Lower etch rates result under these conditions but the selectivity becomes a softer function of bias power which can help in tuning the process. Dilution was found to improve sidewall quality and improve within wafer etch rate uniformity.

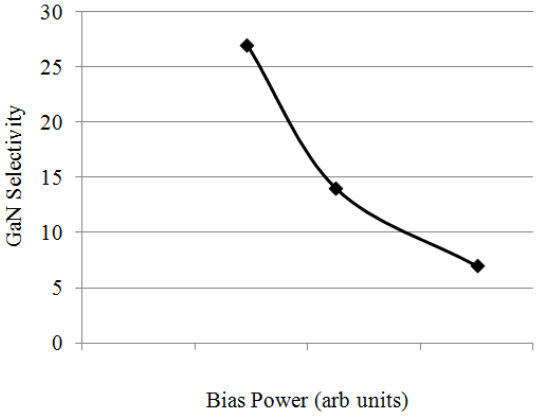

Figure 4 SiC:GaN selectivity ratio vs bias power. SF_6/O_2/He flow rate ratio 10:1:7.

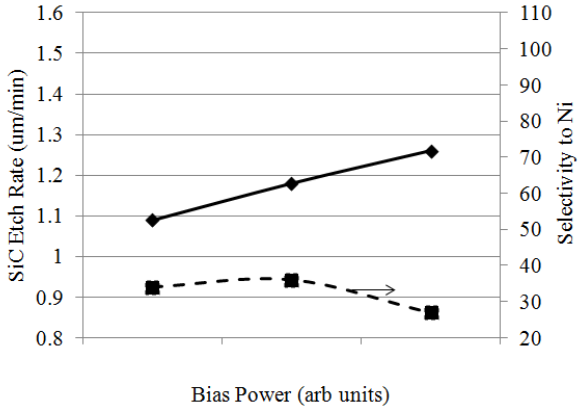

Figure 5 SiC via etch rate and mask selectivity vs bias power. SF_6/O_2/He flow rate ratio 10:1:25.

The next stages of the development saw a move to higher pressure to drive the SiC etch rate and selectivity up whilst maintaining sidewall quality. Figure 6 shows the SiC etch rate and selectivity trends with process pressure.

Table II summarises the process trends for the SiC Via etch tuning.

SEM cross sections for a 100µm deep SiC via etched using a 2 step optimized process stopping on the GaN underlayer are shown in Figure 7. The GaN loss has been measured to be <0.35µm for this process.

Figure 8 shows the via base following GaN etching using a Cl_2/BCl_3 chemistry in the same APS module. This process takes place after the Ni mask has been stripped and the via wet cleaned of polymer. Selective etching of the GaN to the Au metallisation is achieved.

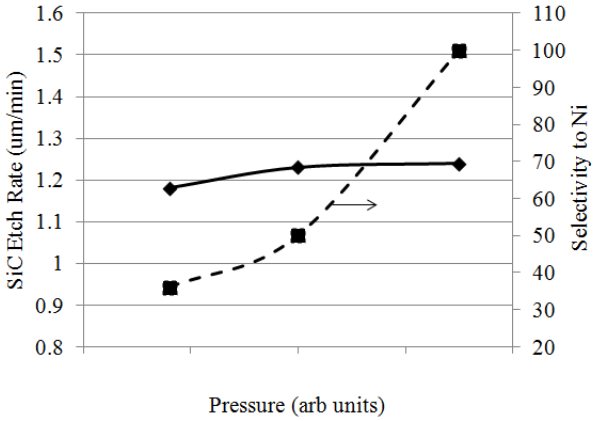

Figure 6 SiC via etch rate and mask selectivity vs pressure. SF_6/O_2/He flow rate ratio 10:1:25.

TABLE II
PROCESS TRENDS FOR SILICON CARBIDE VIA ETCHING

Process conditions	Etch rate	Selectivity to Ni	Selectivity to GaN	Uniformity	Sidewall quality
Bias power	↑↑	↓↓	↓↓	↑ improves	↔
Dilution with He	↓	↓	↓	↑↑ improves	↑ Improves
Pressure	↑	↑↑	↑	↓ Degrades	↑ Improves
Ar addition	↑	↓↓	↓↓	↔	↓↓ Degrades

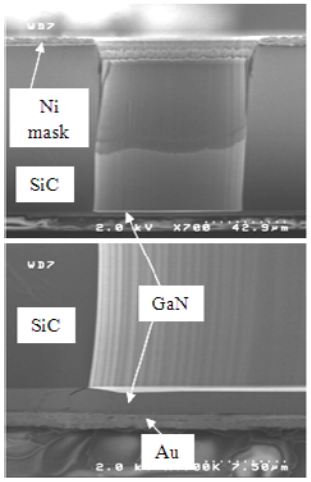

Figure 7 100µm deep SiC via etched to the GaN layer. GaN loss measured at <0.35µm.

End-point traces for the GaN etch are shown in Figure 9. The intensities of the Ga* emissions at 417nm for 2 consecutive wafers show that the total etch times agree within 3 seconds.

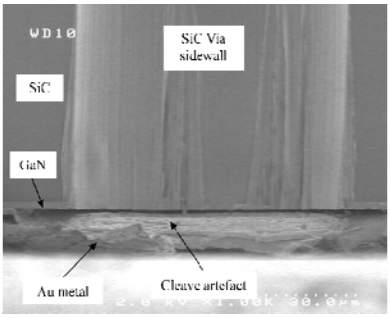

Figure 8 Base of SiC via after GaN etching.

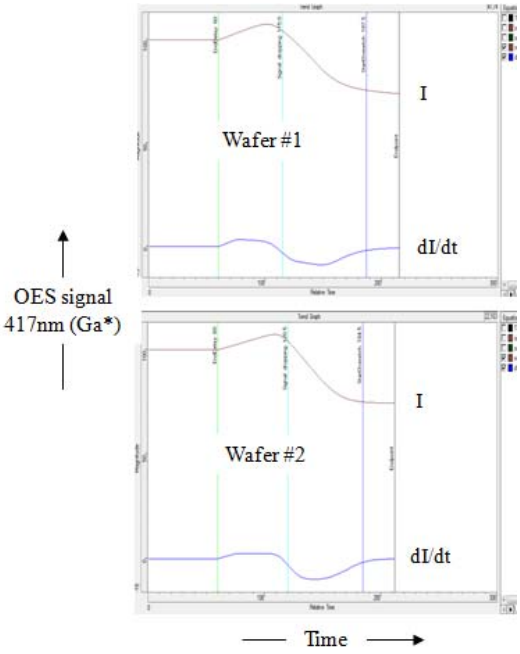

Figure 9 OES end-point traces for 2 consecutive GaN etches stopping on Au.

The ability to clean the via of etch polymer using a 20% HNO_3 solution at room temperature for 15 minutes is shown in Figure 10. The trenching observed at the base of these partially etched vias is typical for an energetic process of this type. The trenching disappears when etching is continued to the GaN layer.

The substrate vias were then coated with a sputtered metal seed layer and electro-plated with Au metal resulting in a nominal via resistanace slightly below 6E-3Ohm.

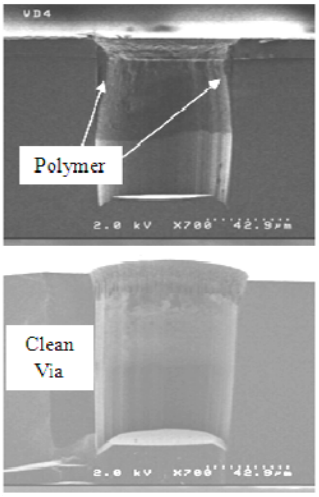

Figure 10 Partial via etches before and after polymer removal in 20% HNO_3 15 minutes.

CONCLUSIONS

A manufacturable SiC back-side via process has been developed for high power device applications. Etch rates >1.3µm/min with cross-wafer uniformities of <±5% have been achieved along with Ni mask selectivity in the range 30-40:1. The use of a unique descum process has resulted in pillar defect levels <1% and the vias are easily cleaned of polymer using HNO_3 solutions. The same module hardware has been used to etch the GaN stopping on Au metal with automated end-point detection control. Via resistances <6E-3Ω have been achieved.

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REFERENCES

[1] V. Bougrov, et al., *Properties of advanced semiconductor materials GaN, AlN, InN, BN, SiC, SiGe.* Eds. M.E. Levinshtein et al., Wiley & Sons, New York pp. 1-30, 2011.

[2] H. Stieglauer, et al., *Evaluation of through wafer via holes in SiC for GaN HEMT technology*, 2012 CS MANTECH Technical Digest, pp. 211-214, April 2012.

[3] J-A. Ruan, et al., *Backside via process of GaN device fabrication*, 2012 CS MANTECH Technical Digest, pp. 215-217, April 2012