SESSION 6a: GaN PROCESS, DEVICE & CIRCUITS

Chairs: Karen Moore, *Freescale Semiconductor, Inc.*
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The GaN Process, Devices, and Circuits session will span a range of topics for GaN process and device technology. One of the highlights of this session is that Cree and WIN Semiconductor will both present their new processes for 0.25 µm optical gate GaN HFET's. The WIN paper will also feature their field plate process that is run with the 0.25 µm flow. These are particularly noteworthy as this is the first time Cree has presented its 0.25 µm production technology, and this is the first GaN paper presented by WIN.

We will also have three papers featuring use of dielectrics in GaN devices and processes. Koehler et al. from the Naval Research Laboratory and Universidad Politécnica de Madrid will discuss their investigation of Atomic Layer Epitaxy (ALE) AlN as a passivation layer for GaN devices, showing improvements in pulsed IV results and better performance than for PECVD SiN passivation. Md. Hasan from University of Fukui will share his results on the effect of sputtered SiN on the current collapse of GaN HEMTs, including the impact of both deposition temperature and anneal temperature on interface trap density. Finally, Osipove et al. from Ferdinand-Braun-Institut in Berlin will discuss their process for using thermally reflowed ZEP520A and CHF_3/SF_6 plasma etching for the formation of slanted gate trenches in SiN. A slanted gate profile has the potential to both improve metal conformality and to improve DC device performance via a slant field plate.