Fabrication technology of GaN/AlGaN HEMT slanted sidewall gates using thermally reflowed ZEP resist and CHF_3/SF_6 plasma etching

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Abstract

In this work we present a technology of slanted sidewall gate fabrication using ICP etching of the SiN_x passivation layer with a thermally reflowed ZEP 520A electron beam resist as etch mask. The influences of reflow time and temperature on structure size and sidewall angle are studied. Furthermore, the dependencies of SiN_x etch rate, RF bias level, and etching selectivity of the SiN_x/ZEP mask on process parameters are determined. A bulk SiN_x etch rate of ~118 nm/min at an extremely low RF bias level of 8 V has been obtained. At these conditions SiN_x/ZEPmask selectivity is 2.5. Gate lengths of 50 to 250 nm at a gate foot sidewall slope of 70° have been demonstrated. Test transistors fabricated on 3" GaN/AlGaN-sapphire wafers show reproducible 50 nm and 100 nm gates with high yield.

INTRODUCTION

Fabrication of gates is the most crucial part in field-effect transistor manufacturing due to its strong influence on device performance and reliability. Currently, the most commonly used technology for GaN-based HEMTs and MMICs is the so-called "embedded gate" process, where the gate metal is deposited into the trench opening etched in a dielectric passivation layer (usually silicon nitride, SiN_x). The semiconductor surface properties at the bottom of the trench opening along with the semiconductor/metal interface quality decide on electrical characteristics and reliability of the transistors. Since trench etching of the dielectric layer also affects the semiconductor surface, the etching process of the dielectric needs to be carefully controlled in order to minimize detrimental effects on device performance [1]. Moreover, the trench etching should provide a trench geometry that allows for conformal metal coverage without void formation. A trapezoidal profile of the gate trench would not only improve homogeneity of metal coverage but also reduce the peak electrical field at the gate edge by forming a slant field plate. It has been shown that slant field plates can reduce dispersion effects [2]. In this work we obtained slanted profiles of the gate structures with dimensions down to 50 nm and a sidewall slope of 70° using resist reflow and SiN_x ICP etching processes. DC electrical results obtained from 2×125-µm-wide AlGaN/GaN HEMTs fabricated on 3 inch sapphire wafers are presented along with the on-wafer distribution of characteristic parameters.

EXPERIMENTAL DETAILS

All preliminary tests were performed on 4 inch s.i. GaAs wafers, while verification of the technology was performed on 3 inch sapphire wafers with the following heterostructure: 1200 nm GaN buffer, followed by 18 nm undoped $Al_{0.24}Ga_{0.76}N$ barrier and a 5 nm thick doped GaN cap layer. All wafers were passivated with 100 nm thick SiN_x films deposited at 345 °C using a Sentech SI500D PECVD tool. The ZEP 520A (Nippon Zeon) co-polymer resist was 50% diluted, spun at 2000 rpm and subsequently baked for 3 min at 115 °C, resulting in a final thickness of ~210 nm. Exposure was performed using a Vistec SB251 electron beam lithography tool with an acceleration voltage of 50 kV and dose of 65 µC/cm². After development the wafers were cut into ~1 cm^2 square samples. Reflow of the resist was performed on a calibrated hotplate at different temperatures and for a series of time intervals. After reflow, samples were etched using Sentech SI500 ICP tool. Size and profile of trench openings in SiN_x were analyzed using scanning electron microscopy (SEM).

REFLOW OF ZEP ELECTRON BEAM RESIST

For the proper mask fabrication by thermal reflow it is essential to obtain sloped sidewalls by rounding the resist profile and to preserve or increase plasma stability of the resist [3]. Recently, for 235 nm thick ZEP 520A-7 on silicon (100) an onset of profile rounding at 145 °C was reported [4]. In the current work, the reflow temperature was varied from 150 to 165 °C with a step of 5 °C. Fig. 1 shows the dependence of average feature shrinking speed on processing time for different reflow temperatures. As can be seen from the graph, for all investigated temperatures average shrinking speed is high at the beginning and it decays nearly exponentially. This kind of resist behavior provides a reliable process window when working in the time range above 10 minutes. In order to maintain high process repeatability all samples intended for etch process optimization were heated for 20 minutes. Fig. 2 shows dependencies of the sidewall slope angle in the resist and in the SiN_x trench, on the reflow process temperature. It is obvious that with

increasing reflow temperature the sidewall slope in the resist mask decreases. This directly transfers into the observed decrease of the SiN_x trench sidewall slope. Using these experimental data, it is possible to estimate process parameters, such as initial resist opening as well as reflow process temperature and duration, which are necessary for the fabrication of a gate trench with the desired length and sidewall profile. For transistor fabrication a reflow regime with a temperature of 155 °C and duration of 20 min was chosen. This regime provides a large process window and smooth edges of resist openings after reflow.

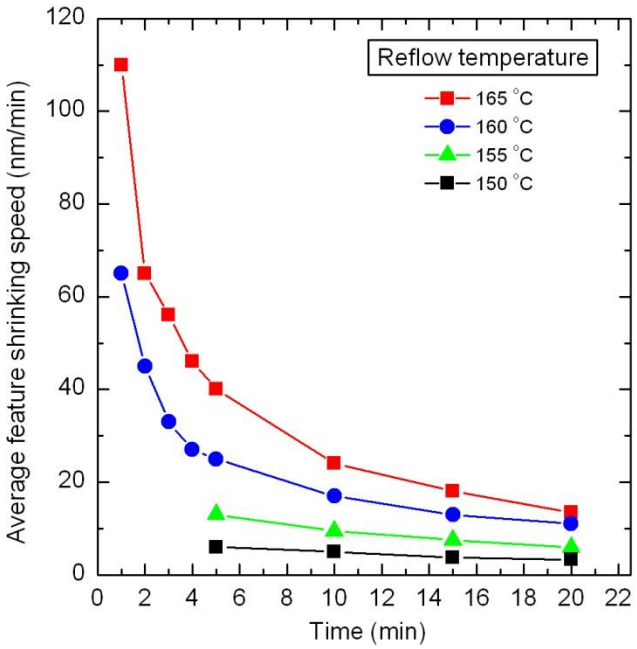

Figure 1. Average feature shrinking speed versus process time for various temperatures.

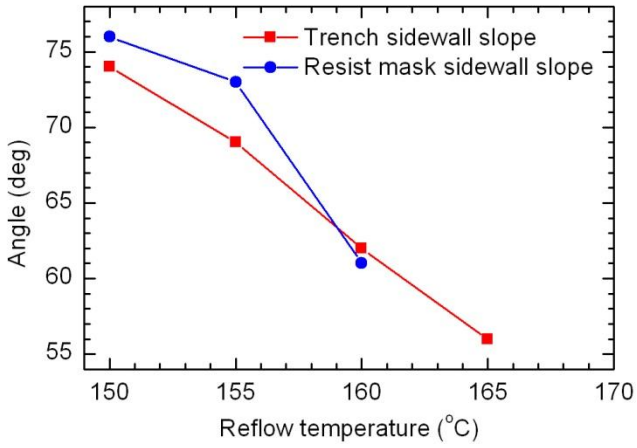

Figure 2. Angle of sidewall slopes versus reflow temperature.

DRY ETCHING OF GATE TRENCHES

Requirements for the dry etch process comprise low bias, high degree of anisotropy and good SiN_x/mask selectivity. In order to meet these requirements, RF power level and process pressure were fixed at the lower limit of the etching tool capabilities (10 W and 2 mTorr, respectively). CHF_3/SF_6 flow ratio and ICP power level were varied to optimize process conditions. As shown in Fig. 3 (a), the etch rate of SiN_x sharply increases with higher ICP power level. At 400 W ICP power the etching of a 100 nm deep trench takes ~30 s. This relatively short process time can deteriorate process repeatability. In order to avoid this, it is necessary to reduce the ICP power level. Figs. 3 (b) and (c) show a strong correlation between ICP power level, process selectivity and RF bias. In terms of bias and selectivity, it is better to use regimes with higher ICP power, but as shown above, there is a limitation by process time. The ICP power level of 300 W allows for a sufficient level of anisotropy of 2.5 and a bias level of 8 V, which satisfies the given requirements. On the left side of Fig. 4 SEM images of the slanted SiN_x trenches are shown that were obtained using the following process parameters: ICP power level 300 W, chamber pressure 2 mTorr, RF power 10 W and CHF_3/SF_6 flow ratio 15. The etch rate of SiN_x for this process was 118 nm/min with a SiN_x/mask selectivity of 2.5 at a bias level of 8 V. Smooth sidewalls and bottom morphology of the trench along with a well-defined opening through the whole trench length were obtained. The right side of Fig. 4 shows SEM images of Ir/Ti/Au gates. It is clearly seen that the first layer of gate metal provides a conformal coverage of the trench region. Thus a reliable separation between the semiconductor or the SiN_x surfaces and the top metal Au is ensured.

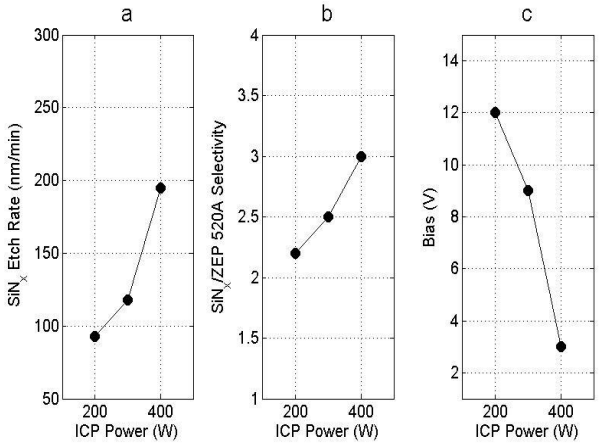

Figure 3. Dependencies of a) SiN_x etch rate, b) SiN_x/mask selectivity and c) bias level on ICP power level for a CHF_3/SF_6 flow ratio of 15.

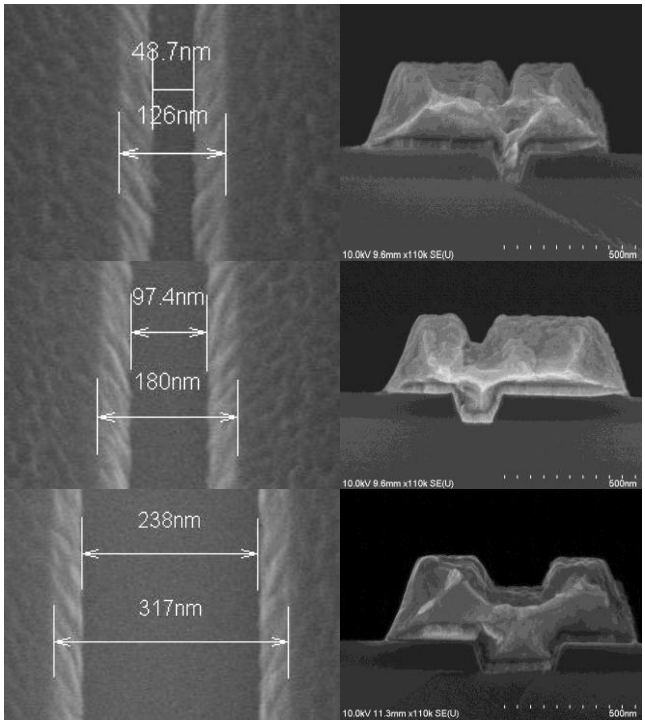

Figure 4. SEM images of different openings in SiN_x (top views, left) and cross sections of gates fabricated in corresponding trenches (right).

ELECTRICAL RESULTS

The compatibility of the developed process was verified with a standard AlGaN/GaN HEMTs fabrication process. Transistors with gate lengths of 50 nm, 100 nm and 250 nm were realized on sapphire wafers with the epitaxial structure described above. It should be noted that the epitaxial structure with a gate to 2DEG distance of 23 nm is not optimal for gate lengths of 50 nm and 100 nm [5]. Strong short channel effects are expected for such a device design. Nevertheless, a verification of the uniformity and yield based on DC characteristics is possible. First, the Schottky contact quality was evaluated for all fabricated gate dimensions (Fig. 6). Measurements of the diode characteristics revealed barrier heights of 1.2±0.1 V together with ideality factors of 1.6±0.2. This is well in accordance to what can be expected from Ir-metal contacts on GaN surfaces [6]. Figure 7 shows DC output characteristics measured for 2×125-µm-wide transistors with gate lengths of 50 nm and 100 nm. The characteristics demonstrate functionality of the gates, as expected the short gate show a well pronounced short channel effect. The fabrication homogeneity of 2×50-µm-wide transistors having gate lengths of 50 nm and 100 nm across the 3" wafer is shown in Fig. 8.

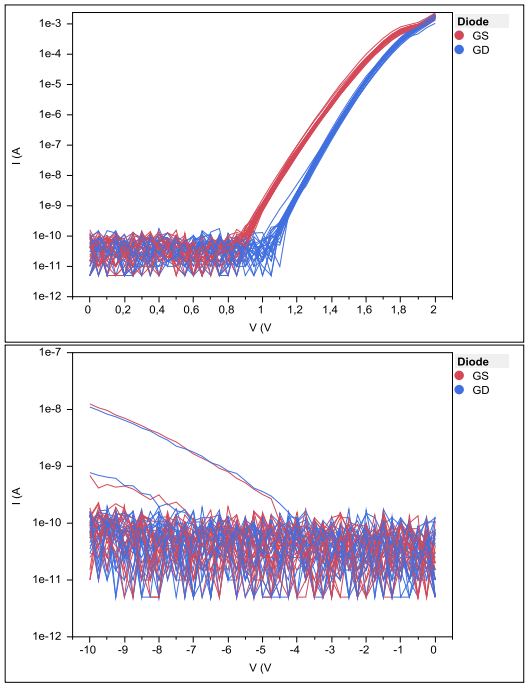

Figure 6. Diode characteristics for forward (top) and backward (bottom) bias conditions (gate-source and gate-drain diodes have been measured)

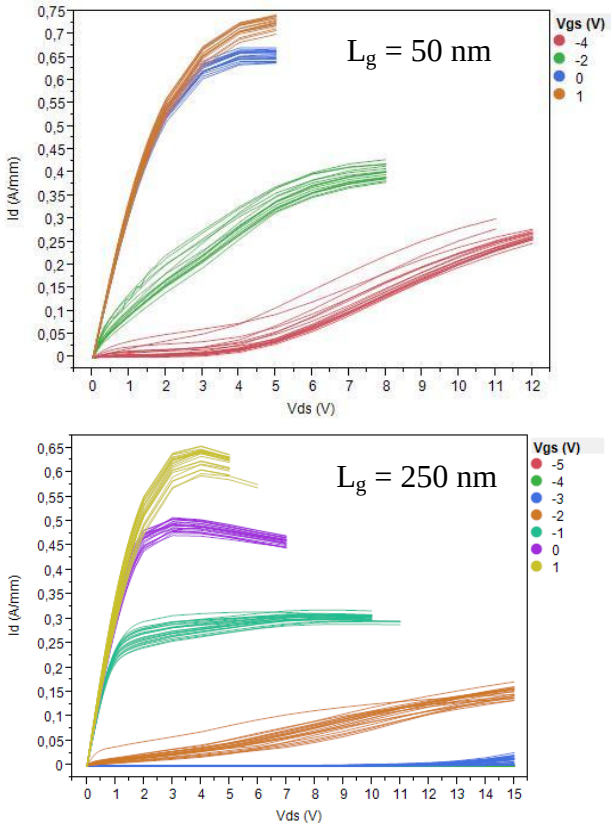

Figure 7. DC output characteristics of 2×125-µm transistors with L_g=50nm, 100 nm and 250 nm

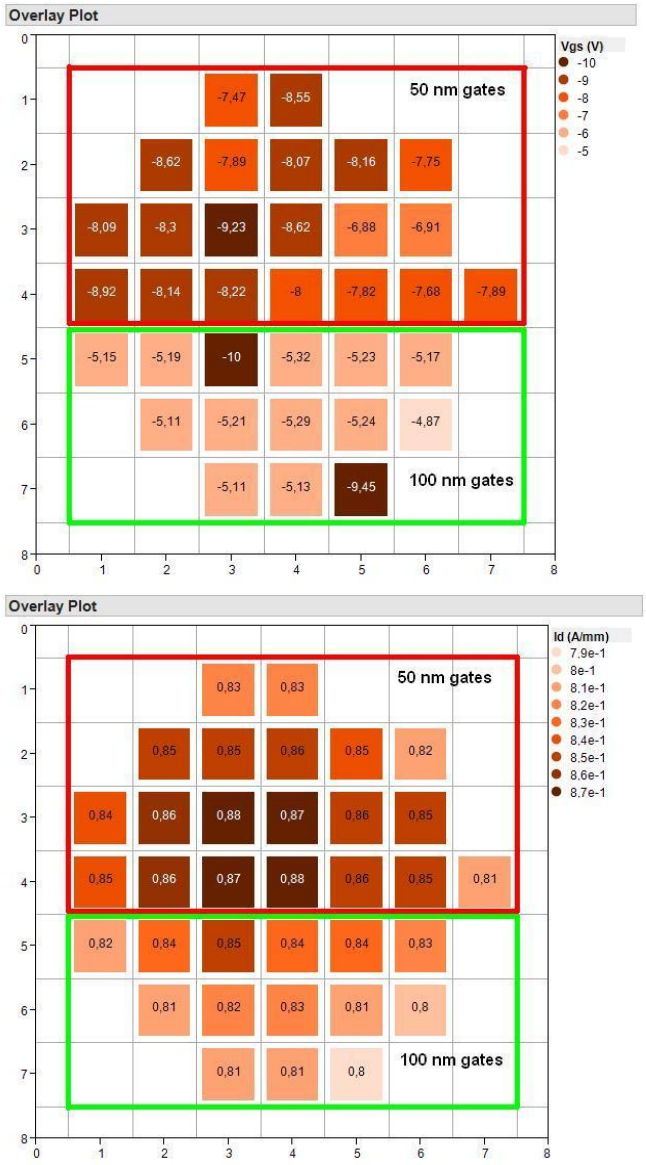

Figure 8. I_{DS_max} (top) and V_{th} (bottom) distribution over wafer area for 2×50-µm transistors with L_g = 50 nm and L_g = 100 nm

CONCLUSIONS

A new process module for defining short slanted gates in AlGaN/GaN HEMTs using resist reflow technique in combination with dry etching has been demonstrated. In detail, reflow of ZEP ebeam resist and subsequent CHF_3/SF_6 based ICP etching of SiN_x was developed. Slanted gates embedded in SiN_x with lengths of 50 nm, 100 nm, and 250 nm and sidewall angles of 70 degrees were fabricated. The optimized process flow is the following:

- reflow of resist mask with initial opening sizes of 125 nm, 175 nm and 350 nm for 50 nm, 100 nm and 250 nm gates, respectively, at 155 °C for 20 min
- ICP dry etching using CHF_3/SF_6 process chemistry
- Ir/Ti/Au gate metal evaporation

The developed gate process module has been verified on AlGaN/GaN HEMTs on 3 inch sapphire substrates. The quality of gate Schottky contacts, the DC output characteristics, and the resulting fabrication yield have proven the suitability of this technology for high frequency GaN MMICs.

ACKNOWLEDGEMENTS

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ACRONYMS

HEMT: High Electron Mobility Transistor
ICP: Inductively Coupled Plasma
RF: Radio Frequency
DC: Direct Current