Device Characteristics Analysis of GaAs/InGaP HBT Power Cells Using Conventional Through Wafer Via Process and Copper Pillar Bump Process

Hsiu-Chen Chang, Shu-Hsiao Tsai, Cheng-Kuo Lin, Tim Hsiao, Steven Chou, Ju-Yung Chen, Pi-Hsia Wang, and Dennis Williams

WIN Semiconductors Corp.

No.69, Technology 7th Rd., Hwaya Technology Park, Kuei-Shan Hsiang, Taoyuan, Taiwan 333
E-mail: andytsai@winfoundry.com, Phone: +886-3-3975999#1512

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Abstract

InGaP/GaAs HBT has been widely used in power amplifier (PA) design for wireless communications. However the self-heating effect and the derivative Kirk effect limit the PA performance to achieve higher efficiency. The copper pillar bump provides several advantages compared to conventional wire-bonding technique such as packaging size shrinkage, removing noise-radiating wires, and more importantly the better heat dissipation. The copper pillar bump can be formed directly on the HBT emitter fingers area through the appropriate thermal shunt inter-connecting metal, which can suppress self-heating and thermal coupling effect. Better thermal dissipating capability can be achieved by copper pillar bump on the top of InGaP/GaAs HBT for better device performance.

INTRODUCTION

GaAs MMICs (monolithic microwave integrated circuits) are widely used in RF modules for portable devices in recent years. In particular, HBT PAs (hetero-junction bipolar transistor power amplifiers) play a key component for 3G/4G LTE and wifi commercial applications.

On the other hand, copper pillar bumps have been used for many years in high-density silicon-based products as a method to create higher-density I/O interconnects from the chip to the lead frame or even to the printed circuit board (PCB) for wafer level packing (WLP). Furthermore, the copper pillar bumps for III-V MMICs [1] not only can save the module size for high-density flip-chip-on-module (FCOM) packages but also own the better thermal and electrical performance compared to the conventional wire-bonding technique.

This paper presents electrical and thermal performance comparisons between conventional InGaP/GaAs HBT power cell through wafer via process and the same device through copper pillar bump process. The electrical measurement includes DC and RF small signal measurement. The thermal measurement includes thermal infrared and temperature varied measurement.

MEASURING METHODS OF ELECTRICAL AND THERMAL ANALYSIS

In this study, both devices are set front-side upward for measuring. Both devices are measured by G-S-G microwave probe with co-planar waveguide pad for DC, RF small signal, and the temperature-varied measurement. The wire-bonding was implemented for thermal infrared measurement. Therefore, the copper pillar can be treated as a floating end.

DEVICE FABRICATION AND FEATURES

This work was done by WIN's 4th generation InGaP/GaAs HBT process [2,3]. The 4th generation HBT process, so called HBT4, includes two interconnection metal layers (M1 and M2) and a thicker SiN layer as the dielectric layer between M1 and M2. A thicker SiN film instead of using Polyimide as dielectric film can provide better mechanical and moisture protection. The thicknesses of two metal inter-connecting layers are 1um evaporated and 4 um plated Au for M1 and M2, respectively. MIM capacitors with unit capacitance of 570 pF/mm^2, stacked MIM capacitors with unit capacitance of 870 pF/mm^2, and thin film resistors with sheet resistance of 50 Ohm/sq can be used for MMIC designs. WIN's copper pillar bump process provides 40 um plating copper and 25 um plating tin cap metal for flip-chip mounting by tin reflow process.

POWER CELL DESIGN WITH CONVENTIONAL WAFER VIA AND WITH EMITTER COPPER PILLAR BUMP

In order to compare the electrical characteristics of both power cell devices through conventional wafer via process and copper pillar bump process, both devices' layouts are set the same except for wafer via and copper pillar as following Fig. 1(a) and Fig. 1(b). Both power cell devices consist of 4

sets of unit cell. One set of unit cell includes three emitter fingers. The emitter fingers of each unit cell are connected in series by emitter thermal shunt metal (M2). The emitter metal of each device is connected to the wafer via and emitter copper pillar bump, respectively. The emitter copper pillar was formed directly on the device's active area and electrically connected to the emitter fingers by its thermal shunt metal or so-called under bump metal (UBM). Both devices are designed with the coplanar waveguide for measuring.

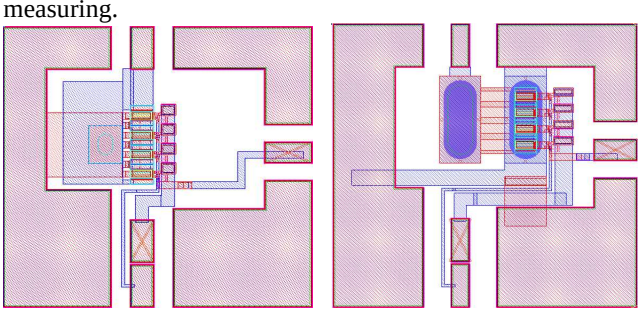


Fig. 1(a) HBT Power cell layout with wafer via process and copper pillar bump process

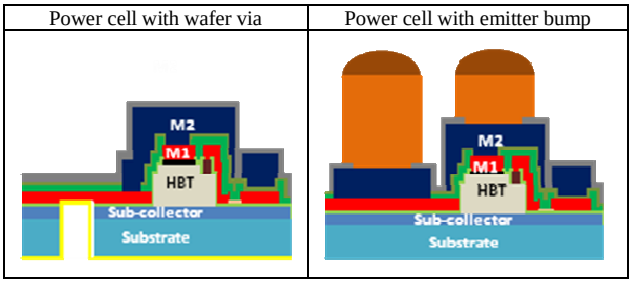


Fig. 1(b) Illustration of HBT Power cell cross-section with wafer via process and copper pillar bump process

Fig. 2 shows the y-axis SEM cross-section picture of HBT multi-fingers power cell with emitter thermal copper pillar bar, which can be achieved by WIN's copper pillar process.

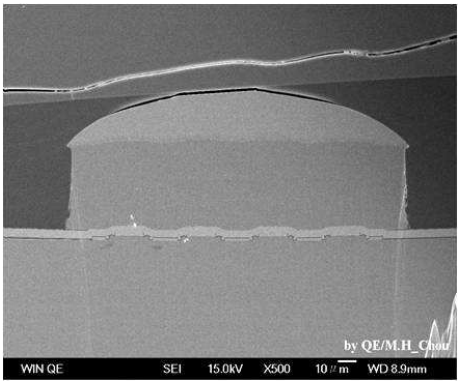


Fig. 2 The cross section picture of HBT with emitter thermal bar type copper pillar

DEVICE DC & RF ELECTRICAL CHARACTERISTICS

Fig. 3 shows the DC I-V characteristics of both power cell devices. The power cell device through copper pillar process shows higher beta value and better thermal dissipation capability than power cell device through conventional wafer via process.

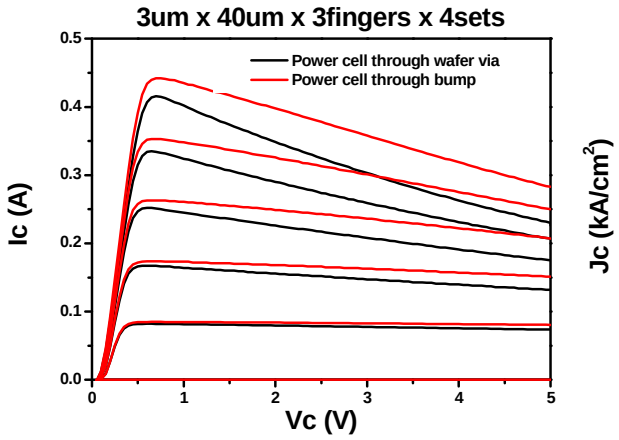


Fig. 3 DC IV Curve comparisons between HBT through wafer via process and HBT with emitter copper pillar bump.

Fig. 4 demonstrates the maximum available gain (MAG) comparison between both devices. The RF small signal measurement condition was set as 900MHz frequency with sweeping collector current (Ic) from 0 to 0.3 Ampere. The result shows that the MAG of the device with copper pillar becomes larger than that of the conventional device with wafer via when collector current exceeds 150mA, which is equal to 10.42 kA/cm^2 of current density. Due to the unit cell consists of 3 emitter fingers, the current will be crowded on center finger instead of outside fingers at high current level, which leads to the non-uniform temperature distribution of conventional device with wafer via. High temperature of center emitter finger makes the device suffers from the base push-out effect, or so-called Kirk effect, earlier at high current level. On the contrary, device with emitter copper pillar not only eases the thermal coupling effect of multi-fingers HBT devices but also postpones the occurrence of Kirk effect at high current densities. The turning point around 150mA in Fig. 4 is the evidence that the device with emitter copper pillar has better thermal dissipation.

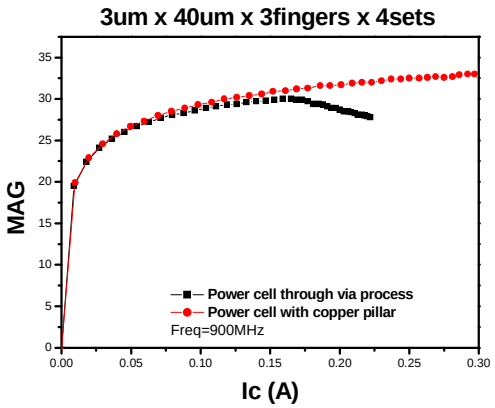


Fig. 4 Maximum Available Gain (MAG) between HBT through wafer via process and HBT with emitter copper pillar bump.

Fig. 5 demonstrates the thermal infrared pictures of both HBT power cell devices with emitter copper pillar bump and with conventional wafer via. The thermal infrared measurement is implemented for checking the emitter surface temperature. Surface of devices are both covered by the thermal shunt inter-connecting metal (M2). The thermal infrared pictures are taken under VCE 3.6V with several collector current levels from 150mA to 450mA.

Table. 1 shows the surface temperature comparison between both HBT power cell devices with conventional wafer via and with emitter copper pillar bump. The highest temperature of both devices appeared at the surface of thermal shunt metal. The surface temperature of device with copper pillar is obviously lower than that of the device with wafer via. The temperature gap between each device becomes larger while the collector current increased. This phenomenon demonstrates that the larger operated current density, the more obvious improvement can be achieved by better thermal dissipation.

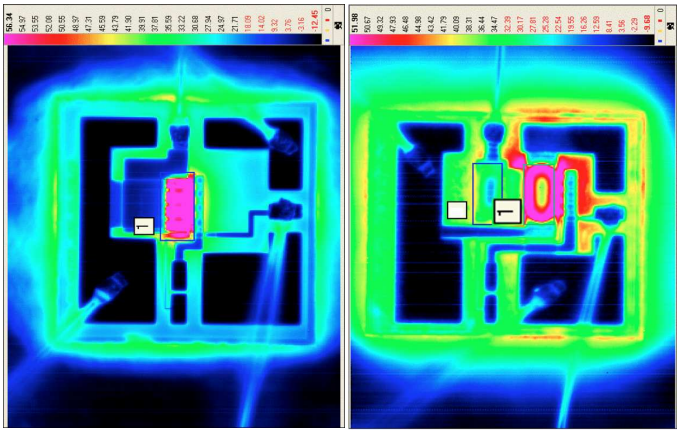


Fig. 5 Thermal infrared photos of HBT power cell devices with wafer via and with emitter copper pillar

TABLE. 1

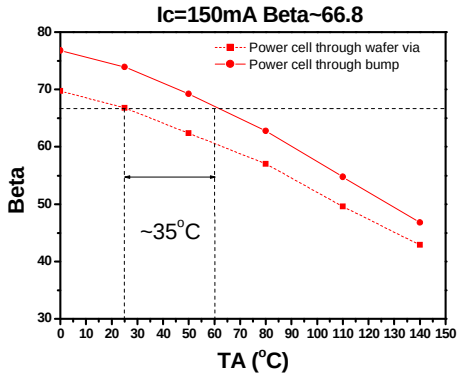
Surface temperature difference extracting by thermal infrared between HBT through wafer via and HBT with emitter copper pillar bump.

Ic at Vc=3.6V	Pdiss	HBT (Through copper pillar)	HBT (Through wafer via)	T_s (Surface temperature) Difference
150mA	0.54W	44°C	58 °C	14°C
250mA	0.9W	69°C	92 °C	23 °C
350mA	1.26W	98°C	125 °C	27 °C
450mA	1.62W	125 °C	165 °C	40 °C

TEMPERATURE DEPENDENCY CURVE OF BETA VALUE

Fig.6 shows the temperature dependency curve of beta value (ß). The measurement system includes the temperature variable chuck, the isolated chamber, and GSG probing on the coplanar waveguide pad. The solid line and the dash line represent the device with copper pillar bump and with wafer via, respectively. The temperature variation range is from 0°C to 140°C. The collector current swept from 150mA to 450mA. The device with copper pillar shows higher beta value than device with wafer via even the chuck temperature exceeded 140°C.

Table.2 demonstrates a simple calculation by the temperature dependency curve of beta. The beta curve (ß) can be used to extract the junction temperature difference between conventional device through wafer via process and device through copper pillar process. The junction temperatures of both devices are assumed the same because of the same beta (ß) value. For instance, the device through wafer via process was operated under 25°C ambient temperature with 0.54W DC output power; meanwhile, the device with emitter copper pillar bump was operated under 60°C ambient temperature with the same output power. Both devices show the same beta value (ß). Thus the ambient temperature difference is 35 °C while beta value (ß) is equal to 66.8. The result shows that the device with emitter copper pillar bump can be operated at higher ambient temperature than device with wafer via with the same junction temperature. The temperature gaps between both devices under 0.54W, 0.9W, 1.26W, and 1.62W DC output power are 35 °C, 40 °C, 48 °C, 55 °C, respectively.



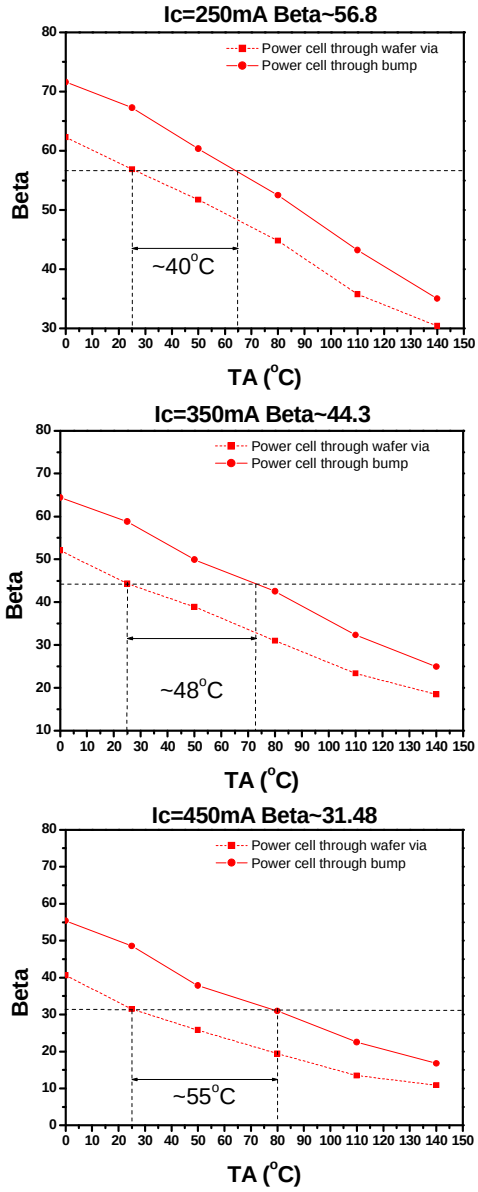


Fig. 6 Temperature dependency curve of beta (ß) at different ambient temperatures (T_A)

TABLE. 2
Temperature difference extracting by temperature dependency curve of beta between HBT with emitter copper pillar bump and HBT through wafer via process

ß (beta)	Pdiss, T_A (Through via)	Pdiss, T_A (Through Cu pillar)	T_A Difference
66.8	0.54W, T_A=25°C	0.54W, T_A=60°C	35°C
56.8	0.90W, T_A=25°C	0.90W, T_A=65°C	40 °C
44.3	1.26W, T_A=25°C	1.26W, T_A=72°C	48 °C
31.5	1.62W, T_A=25°C	1.62W, T_A=80°C	55 °C

CONCLUSIONS

In conclusion, this paper has demonstrated that InGaP/GaAs HBT power cell with emitter copper pillar bump has better electrical and thermal performance than the power cell with conventional wafer via. Better heat dissipation can effectively improve thermal instability of multi-fingers HBTs and suppress the high injection Kirk effect. The thermal infrared pictures show that the surface temperature of device with copper pillar can be effectively decreased. The temperature dependence curve shows that the temperature gaps between both devices under 0.54W, 0.9W, 1.26W, and 1.62W DC output power are 35°C, 40 °C, 48 °C, 55 °C, respectively.

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ACRONYMS

HBT: Heterojunction Bipolar Transistor
PCB: Printed Circuit Board
WLP: Wafer Level Packing