SESSION 7b:
TRAPS & TRANSIENTS
Chairs: Tom Low, *Agilent Technologies*
Chang-Hwang Hua, *WIN Semiconductors Corp.*

This session contains an exciting collection of papers on the important topic of traps. The first is an invited paper by Prof. Roman Engel-Herbert describing and comparing various quantitative methods to measure the interface trap densities (D_{it}) at high-k/III-V interfaces using admittance measurements of MOS capacitor devices. The second paper, a collaboration between Drexel U., and U. of Notre Dame, shifts the focus from III-V's to AlGaN/GaN HEMTs, and presents a study of evolution of strain and defect generation during the HEMT operation using analysis of HRTEM images in order more clearly understand reliability failure mechanisms in these devices. The third paper, a student paper from Ohio State, presents C(V) and I(V) data from ALD/AlGaN/GaN FET-like test structures which show correlations between dielectric-semiconductor charge density, channel mobility and conductivity, and gate leakage currents for very thin (6nm to 18 nm AlGaN layers which will be of interest for future MISHEMTs. The fourth paper, which continues on the AlGaN/GaN HEMT topic, is from the U of Bristol, and presents characterization data and simulation results for deep centers in the GaN buffer beneath the HEMT channel, and their relationship to time dependent HEMT characteristics, including both low frequency noise between 1Hz and 1000Hz, as well as dispersion in transconductance over the same low frequency range. The last paper in the session is from Skyworks MA and presents a pulsed I-V study in which their PHEMT switch technology was optimized to achieve remarkably fast 15nsec off -on transitions by appropriate choice of epi design (varying trap density), gate recess dimensions, pre-passivation treatments of dielectric-semiconductor interfaces, and dielectric deposition conditions.