Low-cost high-efficiency GaN LED on large-area Si substrate

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Abstract

The use of large size Si substrates for epitaxy of nitride light emitting diode (LED) structures has attracted great interest because Si wafers are readily available in large diameter at low cost. In addition, such wafers are compatible with existing processing lines for the 6-inch and larger wafer sizes commonly used in the electronics industry. With the development of various methods to avoid wafer cracking and reduce the defect density, the performance of GaN-based LED and electronic devices has been greatly improved. In this paper, we review our methods of growing crack-free InGaN-GaN multiple quantum well (MQW) LED structures of high crystalline quality on Si(111) substrates. The performance of processed LED devices and its dependence on the threading dislocation density were studied. Full wafer-level LED processing using a conventional 6-inch III-V processing line is also presented, demonstrating the great advantage of using large-size Si substrates for mass production of GaN LED devices.

INTRODUCTION

The use of III-nitride based light emitting diodes (LEDs) is now widespread in applications such as indicator lamps, display panels, backlighting for LCD TVs and computer screens, traffic lights, general lighting, etc. To meet the huge market demand and lower the manufacturing cost, the LED industry is moving fast from 2-inch to 4-inch and recently to 6-inch wafer size. Although Al_2O_3 (sapphire) and SiC remain the dominant substrate materials for epitaxy of nitride LEDs, the use of large size Si provides a potential low-cost manufacturing route because the availability of cheap, large-diameter silicon wafers leads to much lower device processing costs. The main challenges involved in epitaxy growth of high quality GaN on Si are wafer cracking and high threading dislocation (TD) density, due to the large lattice and thermal expansion coefficient mismatch between GaN and Si. We have used AlN nucleation layers and AlGaN buffers to introduce compressive stress to compensate for the tensile stress introduced into the GaN upon cooling from the growth temperature to room temperature. By inserting an in-situ SiN_x interlayer into the GaN layer, the TD density can be reduced by more than an order of magnitude [1]. The stress compensation method and TD reduction method using an in-situ SiN_x interlayer have enabled us to grow flat and crack-free GaN structures on Si with a TD density lower than 10^9 cm^{-2} routinely. The issues involved in the MOVPE growth of GaN-on-Si structures will be illustrated via a comparison with the growth on 6-inch sapphire substrates. The optical properties of InGaN-GaN MQW and LED structures grown on Si are also discussed. Finally, a demonstration of a full wafer-level LED process using a 6-inch processing line is presented to show the great potential of using existing V-III and Si processing lines for sophisticated automated processing for mass production of LEDs, enabled by using large-size Si substrates.

COMPARISON OF MOVPE GROWTH OF GAN-BASED LED STRUCTURES ON 6-INCH SAPPHIRE AND 6-INCH SI

The growth of GaN structures on sapphire substrates is well established and more straightforward compared to GaN growth on Si substrates. Figure 1 shows a comparison of the growth procedure of InGaN-GaN LED structures on 6-inch diameter sapphire (1.33 mm thick) and Si substrates (0.625 mm thick). The structures were grown by MOVPE in a 6x2" Aixtron CCS reactor using a 1x6" susceptor. Trimethylgallium (TMG), trimethylaluminium (TMA) and trimethylindium (TMIn) were used as group-III precursors, while ammonia was used as the nitrogen source. Silane (SiH_4) and cyclopentadienyl magnesium (Cp_2Mg) were used as the source of n-type and p-type dopants, respectively. This reactor is also equipped with an EpiCurve$^{@}$TT sensor, enabling emissivity-corrected real-time temperature and wafer curvature measurement.

The main differences between GaN growth on sapphire and Si substrates are: (1) GaN can be grown directly onto the sapphire substrate, while the growth on Si usually starts with an AlN buffer to avoid "melt-back" etching; (2) No stress management is required for GaN growth on sapphire, while for a Si substrate, a carefully designed AlGaN buffer layer is employed in this case for stress compensation to avoid cracking upon cooling; (3) To reduce the threading dislocation density, a method involving the deposition of a SiN_x interlayer and a 3D to 2D growth mode transition process can be applied to a GaN layer grown on both

sapphire and Si. However, when growing on the sapphire substrate, the TD reduction usually occurs early in the growth based on an intentionally delayed coalescence, while for Si, the GaN thickness for coalescence is limited, necessitating a thinner n-type GaN region; (4) The n-type GaN region, InGaN quantum wells and p-type GaN region are grown on a concave or flat wafer in the case of a sapphire substrate, while the wafer is highly convex bowed in the case of a Si substrate. This means the majority of the GaN structure is under tensile stress when grown on sapphire but under compressive stress when grown on Si.

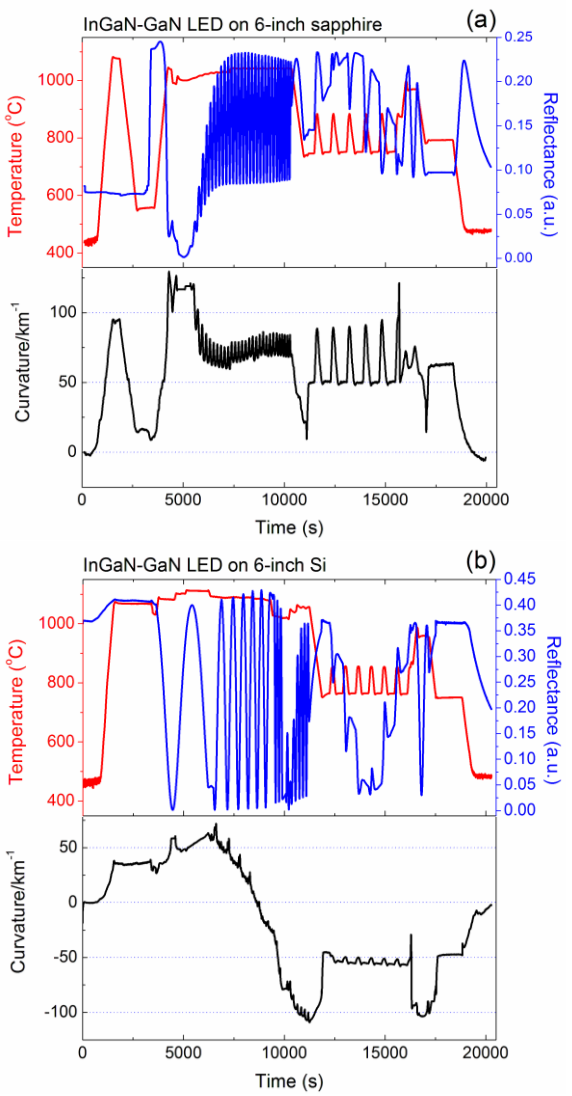

Figure 1 In-situ temperature, reflectance and curvature data collected during the growth of InGaN-GaN LED structures on (a) 6-inch sapphire and (b) 6-inch Si substrates.

From curvature measurements, the LED structures grown on both 6-inch sapphire and Si substrates are flat after cooling from the growth temperature. Thanks to the good stress management, the GaN-on-Si wafer is completely crack-free. The thickness maps of these two LED structures (see figure 2) show good thickness uniformity with standard deviation <1% (no edge exclusion) for both cases. The wavelength uniformity is compared in figure 3 without edge exclusion. Most non-uniformity in the PL wavelength map occurs around the wafer edge, where both the gas flow and temperature change dramatically. This is true for the LED structures on both 6-inch sapphire and Si substrates. The emission wavelength of InGaN-GaN LEDs on 6-inch Si is less uniform compared to that on 6-inch sapphire. This is probably due to the temperature inhomogeneity as a result of the large wafer bow during the InGaN growth on Si substrates. A better adjustment of the heater zones and/or use of thicker Si substrates could help to reduce the wafer bow and therefore improve the wavelength uniformity. The susceptor design can also have a significant impact on the uniformity. In fact, InGaN-GaN LED structures with wavelength uniformity ~1 nm (with 4mm edge exclusion) have been demonstrated on 8-inch Si substrates using a susceptor design optimized for large wafers [2].

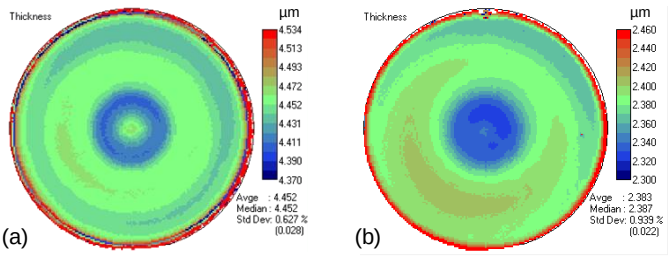

Figure 2 Thickness map collected from InGaN-GaN LED structures grown on (a) 6-inch sapphire and (b) 6-inch Si substrates.

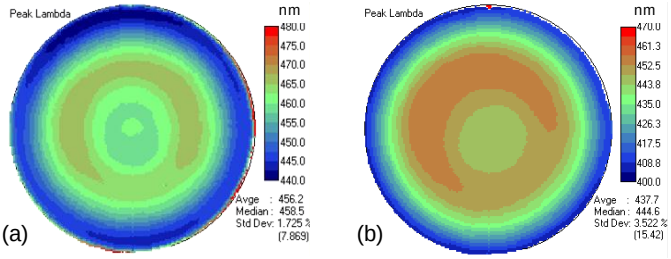

Figure 3 PL wavelength map collected from InGaN-GaN LED structures grown on (a) 6-inch sapphire and (b) 6-inch Si substrates.

OPTICAL PROPERTIES OF GAN-ON-SI STRUCTURES

Several InGaN-GaN MQW and LED structures were grown on Si substrates, with dislocation density varied between $8x10^9$ cm^{-2} to $8x10^8$ cm^{-2} by varying the SiN_x interlayer deposition time from 0 to 240s, similar to that reported in [3]. The TD density is also reflected in the full width at half maximum (FWHM) of x-ray diffraction (XRD) omega peaks, with a narrower peak corresponding to lower TD density [4]. Temperature dependent photoluminescence

(PL) and electroluminescence (EL) measurements were carried out on the MQW and processed LED samples, respectively.

Figure 4 shows the radiative efficiency of the MQW samples using temperature dependent PL measurement. This method is based on assuming 100% internal quantum efficiency (IQE) at low temperatures and the room-temperature IQE is calculated by taking the ratio of the integrated PL intensity at 300K to that at low temperature. The 325nm line from a He-Cd laser was used as the excitation source, with an average excitation power density of 1 Wcm^{-2} [5]. For MQW structures emitting in the 440-450 nm spectral regions, a room temperature PL-IQE value as high as 67% was measured. Higher radiative efficiency was measured in the MQW samples with a narrower GaN (101) omega peak, i.e. a lower TD density. Lower PL-IQE is also observed for the MQW sample emitting at longer emission wavelength of ~485 nm. Despite the difference in carrier injection and loss mechanism under PL and EL operation, similar light output dependence on emission wavelength and TD density was observed on processed LED devices measured using EL, as shown in figure 5 and Ref. [3].

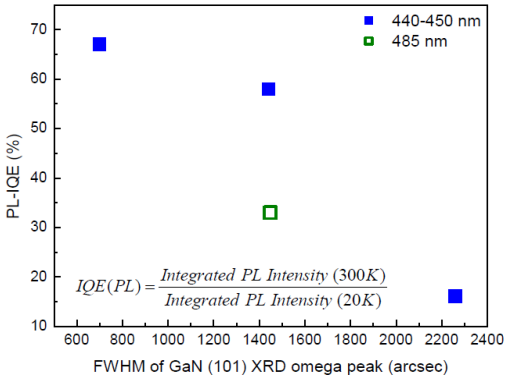

Figure 4 The dependence of IQE on FWHM of GaN(101) omega peak of MQW samples measured by temperature dependent PL.

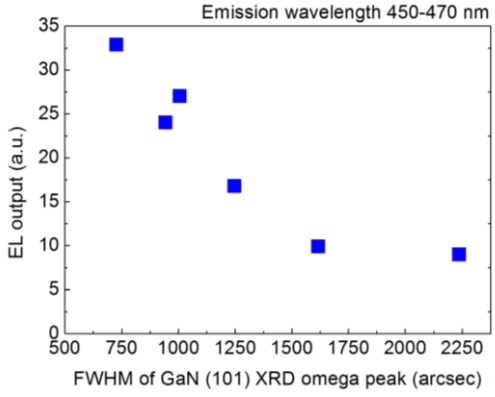

Figure 5 The dependence of light output on FWHM of GaN(101) omega peak for planer LED devices (500 µm x 500 µm) grown on Si substrates, at a drive current of 20mA.

Figure 6 shows the schematic structure of aprocessed LED die of 1mm x 1mm size. No surface roughening or LED die shaping was used in this work to enhance the light extraction. The current-voltage (I-V) and light output (L-I) curves of this LED device are shown in figure 7. At 350 mA drive current, the forward voltage of the LED die is ~4.2 V. The measured light output under 350 mA drive current from the LED die without and with epoxy is 18 mW and 50 mW, respectively. Because the Si substrate is not transparent, only the light emitted from the top surface can escape to be collected in the integrating sphere. A much higher light output is expected after the Si substrate removal and surface roughening.

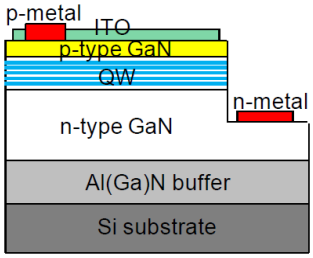

Figure 6 Cross-section of the planer LED devices (1mm x 1mm) on Si.

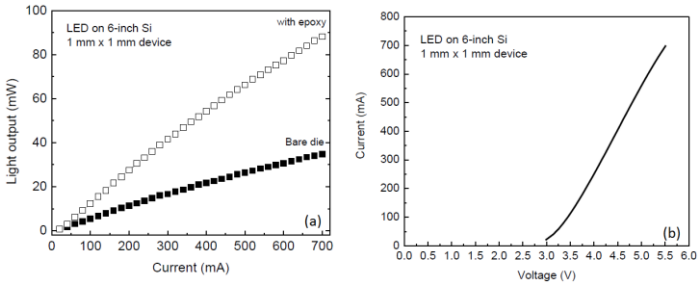

Figure 7 (a) L-I and (b) I-V characteristics of a planer LED device (1mm x 1mm) on Si.

THE DEMONSTRATION OF FULL WAFER PROCESS USING A 6-INCH PROCESSING LINE

One great advantage of using large-size Si substrates for GaN LEDs is the promise of sophisticated automated processing using existing V-III and Si processing lines for mass production. In collaborating with several industrial partners (RFMD UK, QinetiQ, Aixtron and Forge Europa), we have successfully demonstrated full wafer-level LED processing using a conventional III-V 6-inch processing line in 2009. To our knowledge, this was the first such demonstration. Figure 8 shows a picture of a fully processed GaN LED on Si wafer after the n-type, p-type contact deposition, Si substrate thinning from 625 µm down to 100 µm and partial substrate removal. The LED devices can be clearly seen in the close-up pictures shown in figure 8. Because the whole wafer is completely crack-free, LED

9
b

devices with different size and contact geometry design can be processed in a single wafer.

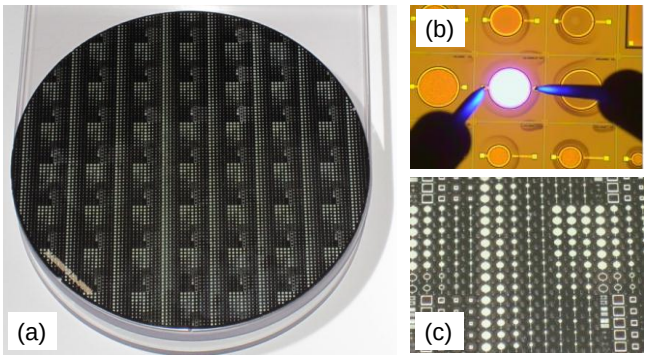

Figure 8 Picture of (a) processed 6-inch InGaN-GaN LED on Si, (b) light emission from one device from this wafer and (c) a close-up picture showing devices of different size and geometry.

There are ~7,500 devices on this single wafer shown in figure 9, with mesa size varied from 50 µm to 1 mm diameter/square. Some devices emit light from the p-GaN side with an overall transparent thin p-type contacting layer, while others emit from the n-side with a highly reflecting p-contact layer. Bright blue light was observed from both types of devices under EL measurement, as shown in figure 9.

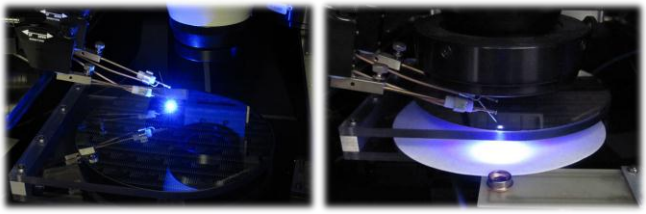

Figure 9 Blue luminescence emitted from an LED device of top-emitting geometry (left) and flip-chip geometry (right) on the processed 6-inch InGaN-GaN LED on Si under EL measurements.

CONCLUSIONS

Crack-free GaN-based MQW and LED structures have been successfully grown on 6-inch Si by using AlGaN buffer layer for stress management. A low TD density of ~$8x10^8$ cm^{-2} was achieved by inserting an in-situ SiN_x interlayer for TD reduction. The growth procedure of GaN on 6-inch Si was compared with that on a 6-inch sapphire substrate to illustrate the challenges of growing GaN structures on Si substrates. The 6-inch LED wafers show good thickness and wavelength uniformity, which can be improved further by using the latest MOCVD hardware design. In terms of optical properties, PL-IQE as high as 67% has been measured from an InGaN-GaN MQW structure grown on a Si substrate, suggesting a high radiative efficiency in the active region. The light output of LED devices shows a dramatic increase with the TD density decreasing from $8x10^9$ cm^{-2} to $8x10^8$ cm^{-2}. Full wafer processing using a conventional III-V 6-inch processing line is presented, demonstrating the great potential of using large-size Si substrates to reduce the manufacturing cost of GaN-based LEDs.

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REFERENCES

[1] D. Zhu, C. McAleese, K. K. McLaughlin, M. Häberlen, C. O. Salcianu, E. J. Thrush, M. J. Kappers, W. A. Phillips, P. Lane, D. J. Wallis, T. Martin, M. Astles, S. Thomas, A. Pakes, M. Heuken, C. J. Humphreys: Proc. of SPIE **7231**, 723118 (2009).

[2] R. Schreiner, A. R. Boyd, O. Rockenfeller, J. Kaeppeler, B. Bchineller and M. Heuken: CS MANTECH conference **333** (2010).

[3] D. Zhu, C. McAleese, M. Häberlen, C. Salcianu, E. J. Thrush, M. J. Kappers, W. A. Phillips, P. Lane, M. Kane, D. Wallis, T. Martin, M. Astles, and C. J. Humphreys: Phys. Status Solidi C **7-8**, 2168 (2010).

[4] D. Zhu, C. McAleese, M. Häberlen, C. Salcianu. E. J. Thrush, M. J. Kappers, W. A. Phillips, P. Lane, M. Kane, D. J. Wallis, T. Martin, M. Astles, N. Hylton, P. Dawson and C. J. Humphreys: J. Appl. Phys. **109**, 014502 (2011).

[5] D. M. Graham, P. Dawson, G. R. Chabrol, N. P. Hylton, D. Zhu, M. J. Kappers, C. McAleese, and C. J. Humphreys, J. Appl. Phys. **101**, 033516 (2007).

ACRONYMS

MQW: Multiple Quantum Well
LED: Light Emitting Diodes
TD: Threading Dislocation
PL: Photoluminescence
EL: Electroluminescence
IQE: Internal Quantum Efficiency