How GaN-on-Si could disrupt the current equilibrium of the booming LED industry

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Abstract

Sapphire and SiC remain the most widely used substrates for GaN epitaxy but many research teams are working on finding better alternatives in terms of performance and total cost of ownership. While GaN as substrate holds some potential on specific high end niches, we consider Silicon the most serious contender as a potential alternative to the widespread use of Sapphire. All major LED makers are exploring the opportunities of transitioning from a sapphire-based technology platform to Silicon-based ("LED-on-Si"). This interest is driven by a potential cost savings of up to 60% at the die level

INTRODUCTION

As the old semiconductor industry goes "if it can be made on silicon it will be made on silicon". Will this prediction turn true for the solid state lighting industry as well? For many years, LED-on-Si has been touted as "the next big thing" in LED manufacturing. However, efforts have so far failed to come to fruition and transform the industry. But in the last 18 months, many established LED manufacturers and startup companies alike have announced impressive results showing that mass manufacturing of LEDs on 6" or 8" silicon substrates might finally be around the corner.

MANAGING TEC AND LIGHT ABSORPTION

The main challenges for the use of Si substrates to manufacture LED stem from the lattice and Thermal Expansion Coefficient (TEC) mismatch with GaN, which are much higher than with SiC and Sapphire substrates. Lattice mismatch results in higher defect densities that are detrimental to performance, and TEC mismatch and high level of mechanical stress in the epitaxial layers causing the wafer to bow during growth and furthermore increasing the potential for reduced yield due to breakage during processing steps to follow. This prevents from growing the thick (> 5 µm) layers needed for LED. In addition, Silicon strongly absorbs light at the typical emission wavelength of GaN LEDs (Blue, Green), thereby suppressing about 50% of the light emitted by the active layers (corresponding to the emission toward the substrate).

Most of these issues have now been solved, and significant improvements in manufacturability and performance have triggered renewed interest in LED on Si.

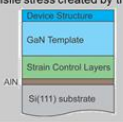
	Stress Management layers	Patterned Substrates	Nano-Column GaN structure
Overview	Include intermediate layers generating compressive stress to compensate for the tensile stress created by the GaN. 	Create deep trenches in the Si substrate in order to promote isolated GaN growth on silicon island and avoid accumulation of tensile stress on the entire wafer. 	Grow vertical nano scale and discontinuous LED structures. The strain is localized at the base of the nanowires, and thus doesn't bend or crack the wafer. 
Benefits	•The full surface of the wafer is available •Can be grown in situ in the MOCVD reactor	•Good reproductibility.	•Possibly compatible with any wafer size
Drawbacks	•Difficult to control, reproducibility	•Reduces useable wafer area •Requires additional lithography/masking and etching pre-processing of the wafer.	•LED Processing (contacts, electrodes, etc.) might differ significantly from standard process
Comments	Typical stress release structures comprise multilayers of GaN / Low temperature AlN layers	This techniques is often combined with stress management layers	Still in development, processing and performance not proven yet
Example	Azzurro, Lattice Power, Bridgelux, Samsung, Lumileds, Sanken, Translucent, Rose street Lab, IMEC	Lattice Power, Photonics Technology Center (Hong Kong)	GloAB, HelioDEL.

FIGURE 1: MAIN SOLUTIONS TO GROW LED ON SI SUBSTRATE

THE MAIN INCENTIVE FOR MAKING LED-ON-SI IS COST, NOT PERFORMANCE

The potential advantage of LED on Si is cost, not performance. The key conditions for LED on Si to succeed are:

1. Must equal LED on Sapphire performance
2. Must reach similar manufacturing yields
3. Must be compatible with CMOS, ideally on 200 mm

The major incentive for a transition to Si wafers for LED manufacturing is the possibility to process the epiwafers in 150 mm or 200 mm fully depreciated and highly automated (efficient) CMOS fabs.

If technology hurdles are cleared, LED on Si will be adopted by some LED manufacturers, but will not necessarily become the standard. A single large CMOS fab could supply worldwide LED demand for years to come. As a result, massive adoption of LED on Si would dramatically change the landscape of the front-end LED industry. It would facilitate the emergence of new or smaller players who currently don't have access to the capital needed to become major players in the industry, and could also entice vertically integrated LED makers to abandon in-house chip manufacturing because of higher production costs.

All major LED companies are investigating LED on Si, but only 3 (Bridgelux / Toshiba, Plessey and Lattice Power) have so far committed to the transition and Osram has just announced the building of a pilot line.

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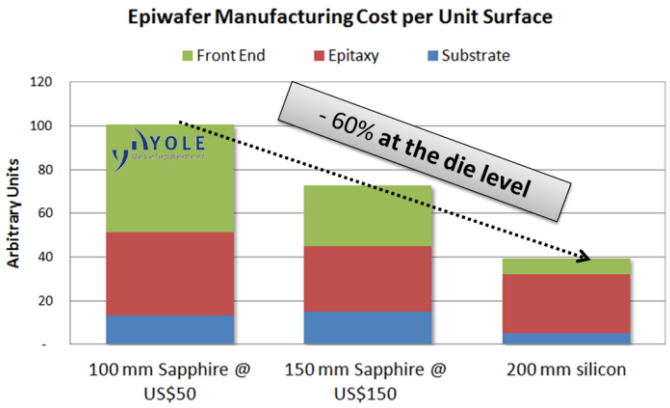

FIGURE 2: LED-ON-SILICON: POTENTIAL COST BENEFITS

The simulation shows a potential cost benefit of 60% at the die level, with the bulk of the savings coming from the processing in CMOS fabs.

Proponents of a transition to Si (Bridgelux / Toshiba, Lattice Power, Azzurro) claim similar cost benefits of about 70% by switching from 2" sapphire to 6" or 8" silicon.
With the die typically representing 55% of a packaged LED cost, such cost reduction could translate into an immediate 30% improvement in the packaged LED cost. While significant, this is put in perspective with the DOE packaged LED cost reduction roadmap, and historical packaged LED price reduction trends. LED-on-Si could help reduce LED lighting COO but is not a mandatory step for the industry to reach its cost targets.

CMOS COMPATIBILITY IS MANDATORY

Most of the cost benefits of an Si platform stem from the ability to use fully depreciated and highly automated CMOS fab. It is therefore critical that LED epiwafers can be processed in such fabs without requiring a major retrofit and additional capex.

Table 1 illustrates the main challenge for the processing of LED epiwafers in a CMOS Fab.

	Diameter	Wafer Bow	Wafer Thickness	Contamination	Wafer Reflectivity
	6" minimum ≥8" better	< 50 – 60 µm	725 µm (200 mm wafers)	No gold	Reflective surface
LED on Al_2O_3	Available but (still) expensive	Can be managed with thicker wafers	6": 1 to 1.3 mm Not compatible + too heavy	Used for bonding and other layers	Incompatible with equipment sensors
LED-on-Si	Available, low cost	OK with strain management	> 725 µm: can be thinned down	Used for bonding and other layers	OK

TABLE 1: CONDITIONS OF SUCCESS TOWARD CMOS COMPATIBILITY

Gold contamination remains a major issue. LED manufacturing processes use gold for various metallization layers. While development of Au-free LED structures and processes is being investigated, it is most likely that LED epiwafers will have to be processed in 100% dedicated CMOS fabs.

In order to manage the bow during epitaxy, the thickness of the wafers used for LEDs is higher than Si SEMI standards. In order to be processed in CMOS fabs, LED-on-Si epiwafers therefore need to be thinned down. Other process steps specific to LEDs would require some level of modification and re-tooling in CMOS fabs. These include wafer probing (optical tests), and dicing. Overall, we estimate that a standard CMOS fab should be 60%-80% compatible with LED manufacturing. This means that the assumption of using a 100% fully depreciated CMOS fab for LED-on-Si manufacturing might be slightly over optimistic.

CONCLUSIONS: SILICON, WILL IT HAPPEN?...MAYBE

Transition to Si is definitely a cost game ($/lumen), not a performance driven choice. Silicon enables 200 mm in fully depreciated CMOS fabs but process yields and fab compatibility remain issues. Moreover, the economics that are true today may be totally wrong tomorrow as incumbent Sapphire substrate market price is declining very fast, on a daily basis. Thus, GaN-on-Si adoption becomes a race against a moving target: Sapphire. The next 2 years will be critical as sapphire 6" price erosion and 8" emergence may fundamentally disrupt today's equations.

REFERENCES

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ACRONYMS

CMOS: complementary Metal Oxide Semiconductor
COO: Cost of Ownership
DOE: Department of Energy
GaN: Gallium Nitride
LED: Light Emitting Diode
TEC: Thermal Expansion Coefficient