Heterointegration technologies for high frequency modules based on film substrates.

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Abstract

System integration technology requires multi-functionality and in many cases energy autarkic systems, very cost-efficient or open form factor solutions. Integration in plastic or foil substrates by a flex-to-flex integration concept shows the potentially free form factor which allows placing of film based systems on curved surfaces or in housings of very low thickness. Such technologies are not limited to flexible applications. They are available for optimized rigid modules and improve the heat sink by thinning and foil handling of transceiver chips or power devices. Thin semiconductor technologies are not limited to silicon, enabling also heterointegration with compound semiconductors. Meanwhile it is possible to integrate high frequency interconnects and printed passives in plastic foil and thin silicon interposer. Possible application scenarios are large area electronics in ceilings panels of cars or mobile communication systems for the "internet of things and humans".

INTRODUCTION

Flexible organic and large area electronics (FOLAE) and in particular foil handling and integration technologies made a large progress just in the last years [1, 2].
In the meanwhile it is possible to hetero-integrate full systems in a foil with organic integrated circuits and PV, display, passive components, flexible battery, thin silicon IC, as well as printed sensors and actuators. The combination of several of these components will be the key to product application in near future [1]. The main focus is no longer only miniaturization but also modular solid state technology development with the aim of heterogeneous integration and the development of smart low power, energy autarkic multi-functional systems [2].

HETEROGENEOUS INTEGRATION OF FOIL SYSTEMS

With components manufactured by optimized modular process technology heterogeneous integration of functions from different technology environments like wafer or foil substrate will become possible and a significant advancement in functionality, flexibility and profitability will be reachable [2]. Modular integration of highly functional film based electronics requires some specific assembly and test techniques to be combined in a technology line [2]. Therefore the manufacture of fine line metal patterns (line /space geometries below 20µm) see fig. 1 on film substrates, preferably to be done by cost-effective roll-to-roll technology has been combined with technologies for handling and lamination of film based sub-modules.

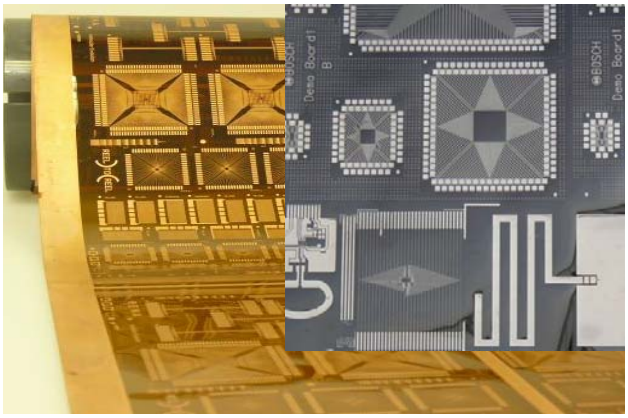

Fig. 1: High resolution copper patterns on roll-to-roll plastic film, capable for antenna, waveguides and IC chip integration on film substrates and compatible with roll-to-roll processing.

A technology has been developed for reliable electrical interconnection between vertically stacked film layers including through-hole via technologies for foil stacks. The manufacture and handling of ultra-thin and flexible integrated circuits has been combined with placement of SMD type passive components by integrated printed passives which do not affect bendability and the overall flat shape. Last not least the test and evaluation of the reliability of the flexible system under mechanical bending and relevant environmental stress has been performed. The corresponding process flow for manufacturing of fine line metallization in film substrates is depicted in Fig. 2. Applying this technology it is possible to integrate RF wave guides in PI and LCP foil technologies showing very promising performance. In order to compare the performance of high-frequency wave guides manufactured in film substrates two technologies called A (commercial) and B (Fraunhofer EMFT) technology have been compared.

10 b

The commercial technology A applies a subtractive layer definition. This means that the metal layer first is rolled on the substrate completely covering the substrate (copper clad). A thin layer of black copper oxide (CuO) increases the adhesion to the substrate. After a mask process the metal is etched in order to from the structures. The EMFT reel to reel technology B applies a pattern plating process for the metallization. It starts with sputtering an adhesion layer of few nm Cr followed by Cu with a thickness of 500 nm. A reel-to-reel lithography using a dry resist defines the metal pattern. A standard acid Cu bath is used for the electroplating process step.

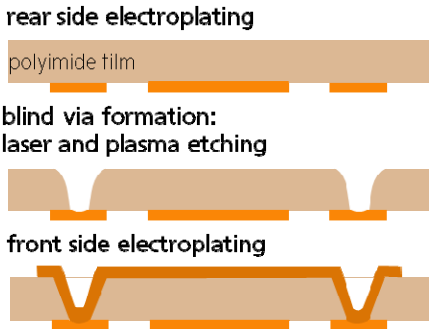

Fig. 2a: Process flow of the interconnect technology on flexible foil (polyimide). In the lower part of the drawing the cross-section of the via is depicted. The same technology is applied to define the wave guides.

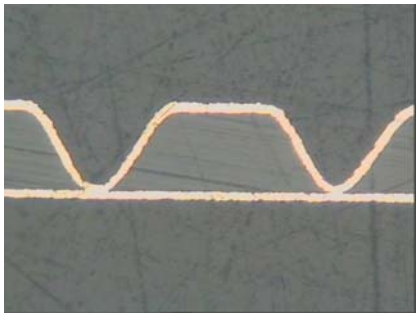

Fig 2b: cross-section of the through-foil interconnect, the PI foil has a thickness of 50µm (distance between the two copper layers). The via metallization is electroplated. The same technology is applied to define the wave guides.

The following process steps include resist stripping and etching of the Cr/Cu plating base. In order to investigate the differences between the two technologies in more detail Fig. 3 shows the cross sections (FIB Focused Ion Beam preparation) of the metal lines for the investigated technologies. Technology A shows a Ni passivation layer of 3 µm. Since Ni is a high permeable element this layer will influence the RF behavior for frequencies higher than 0.5 GHz. Furthermore the definition of side walls is less accurate than for technology B. The extracted average overall height of the metal layer was 12.8 µm (PI)/11.1 µm (LCP) ±1 µm for technology A and 8 µm ±3 µm for technology B. The even more important difference between the technologies is found at the interface between the substrate and the metallization. The structures of the process B show a much lower roughness at the interface than the technology A elements. The AFM scans of the substrate surface showed that the roughness of technology A is by a factor of 100 higher in comparison with the substrate applied for technology B. The roughness of the Cu interface (Figure 4) also partly reflects this difference.

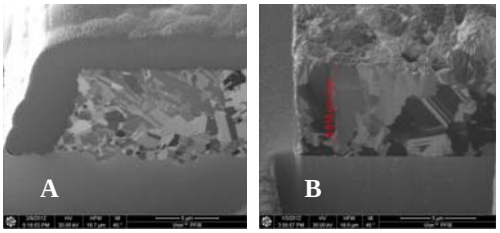

Fig. 3: Cross sections (FIB Focused Ion Beam preparation) of the metal lines for technologies A (left) and B (right).

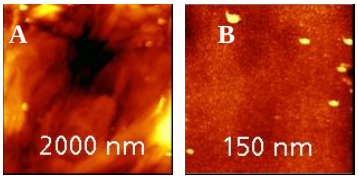

Fig. 4: AFM scans of the Cu interface showing the roughness of the surface for technologies A (left) and B (right).

The roughness of the metal interface to the substrate is in the range of 2 µm for technology A and thus far higher than for technology B showing a roughness in the range of 150 nm. For frequencies higher than 1 GHz the skin depth is lower than 2 µm. Thus, for technology A the roughness will significantly influence the RF behavior. In the range up to 60 GHz the skin depth decreases to approximately 260 nm which is still above the roughness determined for technology B.

RF MEASUREMENTS

The investigated test sheets included variations of micro strip lines (MLIN) and backside grounded coplanar waveguides (BGCPW). As an example Fig. 5 shows the S21 comparison of two BGCPW variations for the applied technologies on PI substrate. Having a 3 dB bandwidth of 40 GHz the structures of technology B exceed the 3 dB-bandwidth of the technology A structures by a factor of 4. The main reason for this increased bandwidth is the much lower roughness at the interface between the metallization and the substrate. Furthermore the technology B does not show a Nickel/Au coating of the copper metallization which introduces an additional inductance at higher frequencies for the technology A (skin effect) [4]. In addition, due to the coplanar layout the proximity effect concentrates more

current in the side walls of the metal traces. Thus, for the structures of technology A the higher roughness of the side walls leads to an increasing attenuation with decreasing gap width. The structures of technology B with a well-defined geometry of the side walls show no significant effect on the gap distance.

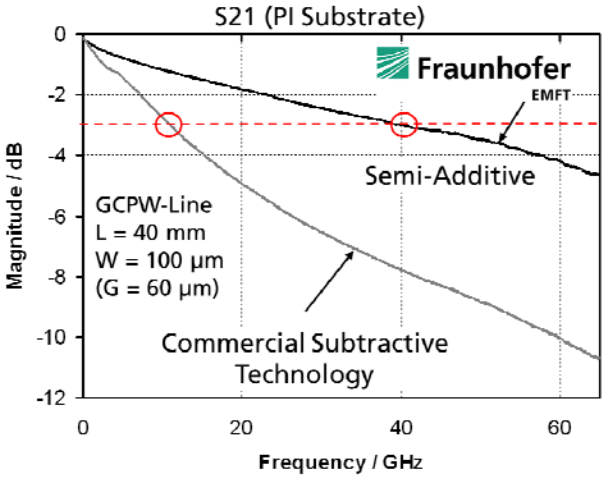

Fig. 5: S21 characteristics of BGCPW variations for both investigated technologies.

System Application

A new process sequence "pick & laminate" has been developed in the frame of the EC INTERFLEX project for vertically stacking of film based sub-modules. This technique allows stacking of multi-layer foil modules of different size and without restrictions on the target position based on adhesive tapes. An alignment accuracy of 50 µm could be confirmed repeatedly. Electrical interconnects have been realized by jetting of silver filled adhesives into the laser drilled through film vias which typically show diameters of 500 µm. The resistance of vias is within 20 – 40 Ω per daisy chain corresponding to 36 via holes. Performed reliability tests of double layer film assemblies with electrically active through film vias showed very promising results. A first decrease of the electrical performance has been observed at a bending radius of 5 mm and the daisy-chains of vias changed their resistance by roughly 5 % only. Screen printed resistors (based on carbon paste) were homogenously integrated on the circuit foils (range 100 Ω to 10 M Ω, uniformity +/- 6.8 %). No changes in resistivity were found after bending tests (1000 cycles, radius 2.5 cm). Humidity tests (85 °C, 85% r. h., 110 h) were additionally performed after mechanical bending. Here the printed bare resistors (no passivation layer on top) changed their resistance by roughly 6 %. In order to be able to integrate specific microelectronic functionalities which are already available as silicon based integrated circuits, such IC devices must be made available at a thickness of 20 – 30 µm which means they are already thinner than a single sheet of plastic film. Also, such thin semiconductor i.e. silicon devices are highly flexible and still show sufficient mechanical robustness for secure handling and assembly.

New chip assembly technologies are supposed to play a key-role for film based electronic systems. Currently handling and assembling of ultra-thin bare dies is limited, soon thin dies will self-assembled on foil substrates will be available in the configuration of a "thin chip foil package" they become mechanically robust and can be handled like other electronic components. Such technologies are also available for compound semiconductor thin devices. In spite of their higher brittleness compared to silicon such thin film handling and flexibility is only a question of the right thickness.

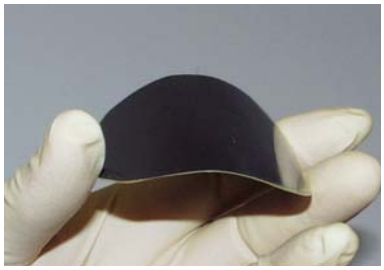

Fig. 6: Flexible GaAs wafer thinned down to less than 30 µm thickness [5].

As an example for a flexible sub-module on film with an integrated ultra-thin IC a transceiver chip was selected for radio frequency (RF) data transmission in the Interflex project. This RF sub-modul was prepared on polyimide film substrate. Product wafers were thinned to some 25 µm and thin dies have been attached to the film circuit by ACA adhesives. Figure 7 shows such RF module; the thin die is placed under a cover sheet in the center. The thick SMD components on the RF film-module clearly show the dramatic difference in thickness between the ultra-thin IC component and assembled passives (capacitors and quartz). The picture underlines the demand for thinner passive devices which can be integrated on plastic films. Such foil technologies may also be used for thinning down and handling of compound semiconductor devices aiming much better cooling or co-integration with other technologies even in for rigid chip modules [5]. Thin GaAs wafer thinned down to less than 30µm (see figure 6), in-spite of its brittleness the GaAs is flexible or bendable as similar as silicon, but in a relation to the brittleness/elasticity, the GaAs bending radius is still approximately 10 times larger before crystal damage occurs. In other words silicon is 10 times more bendable at the same thickness compared to GaAs. The application of thin film semiconductor interposer technologies for packaging of high frequency devices on specifically structured silicon wafer substrates offers several additional advantages for the integration of systems in multi-layer film substrates: high thermal conductivity of the base substrate, highly accurate definition of conducting lines and intermediate spacing and very smooth surfaces and interfaces. All together this results in a 3D-package solution for which the electrical performance can be simulated before

manufacture of the system. Possible substrate configurations comprise cavities for embedding of thin dies (for instance RF GaAs devices) and through silicon via (TSV) contacts for interconnection of "ground patterns".

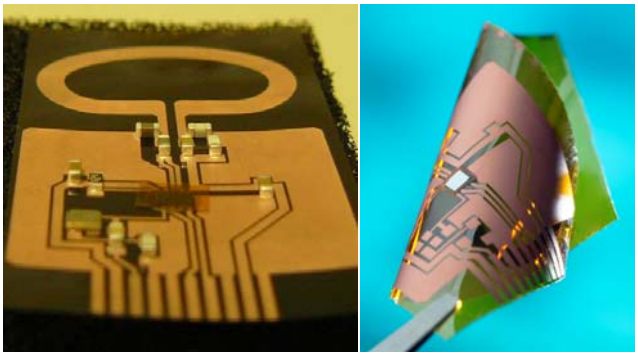

Fig. 7: RF sub-module based on flexible films: the 25 µm thin transmitter chip is placed below a cover film in the center of the module; the thick passives are standard SMD components. A replacement of resistors by printed technologies is close to reach with tolerances of roughly 6%.

Fig 8 shows a SEM picture of a 70 µm deep cavity prepared in a silicon wafer surface, completely covered by a thin gold layer and the end pattern of a "signal line" surrounded by "ground" areas [6]. Fig 8 (top/right) shows a detailed view into a 50 µm wide and 70 µm deep gold plated TSV. The highly accurate definition of all edges and dimensions is the key for high electrical HF performance.

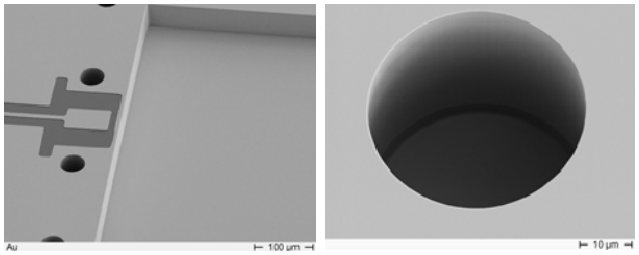

Fig. 8: (right) ground-signal-ground (GSG) interconnection line between two cavities prepared in a silicon substrate. Details are shown Fig. 8 (top/left): end of the micro stripline at the edge of the cavity; Fig. 8 (top/right): through silicon via (TSV).

In the Fig. 8 (right) the gold-plated ground-signal-ground (GSG) interconnection line is depicted connecting between two cavities prepared in a silicon substrate. Furthermore, integrated systems of several chip devices can be designed and prepared as well.

CONCLUSIONS

The status of film heterointegration technologies has been introduced and linked with wave guide manufacturing in film substrates, silicon RF interposer and handling of thin semiconductor substrates. Full system hetero-integration for products is in reach for foil substrates merging classical board and RF technologies with organic integrated circuits and PV, display, passive components, flexible battery, thin silicon IC, as well as printed sensors and actuators. It should be mentioned that such foil technologies can also be applied for rigid modules to reduce the topography or to improve the heat sink and for flexible and open form factor applications. The combination of several of these components is demonstrated applying RF wave guides in film substrates enabling autarkic multi-functional wireless systems for product application, but also for new semiconductor handling and packaging technology. This enables the hetero-integration of different technologies like compound semiconductor with silicon technologies and MEMS and shows the potential to improve form factor, performance (like cooling, etc.) and cost.

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ACRONYMS

FOLAE: Flexible organic and large area electronic
TSV: through silicon via