A Study on Al_2O_3 Deposition by Atomic Layer Deposition for III-Nitride Metal-Insulator-Semiconductor Field Effect Transistors

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Abstract

We studied the impact of atomic layer deposition (ALD)-grown Al_2O_3 deposition conditions on AlGaN/GaN metal-insulator-semiconductor field-effect transistors (MISFETs) using a two-level fractional factorial design of experiments. Three responses, including the threshold voltage shift, the gate-to-source leakage current and I-V hysteresis are studied to understand the effects of each processing variable and interaction. An optimal recipe was then determined to achieve a drain-current hysteresis of less than 0.5V with a gate leakage current of less than 1pA/mm for AlGaN/GaN MISFETs on silicon substrates. The drain-to-source breakdown voltage is also greater than 170V, corresponding to lateral breakdown field of > 1.1 MV/cm.

INTRODUCTION

III-N metal-insulator-semiconductor field-effect transistors (MISFETs) are advantageous when compared to III-N high electron mobility transistors (HEMTs) in term of larger gate voltage swing and lower gate leakage. Different high-*k* dielectrics have been incorporated using different deposition techniques, such as MOCVD and pulsed laser deposition [1,2]. Al_2O_3 film deposited by the atomic-layer deposition (ALD) technique is one of the promising approaches for MIS devices because of its larger bandgap and better thermal stability than ZrO_2 and HfO_2. Several reports have indicated that the ALD deposition and the post-deposition annealing condition have significant impact on the performance of III-N MISFETs [3-5].

In this work, we conducted a designed experiment by exploring six variables that are relevant to the ALD Al_2O_3 gate dielectrics in III-N MISFETs using a fractional factorial design approach. The most significant variables and interactions were studied for three selected output responses, i.e., threshold voltage (V_{th}), gate-to-source (GS) diode leakage and I-V hysteresis. Based on the results, an optimal processing condition were found to achieve threshold voltage shift (ΔV_{th}) < 5 V, GS diode leakage < 1 pA/mm and I-V hysteresis < 0.5 V on 15nm Al_2O_3 gate dielectric.

DEVICE FABRICATION AND EXPERIMENT DESIGN

The study was performed on a home-made ALD tool installed at the Nanotechnology Research Center at Georgia Tech. A schematic diagram of the ALD system is shown in Figure 1. The system consists of two precursors, trimethylaluminum (TMA) and water (H_2O), controlled by ALD pulse valves. N_2 is used as the carrier gas in the system. All the adjustable parameters, including the deposition temperature (variable n_3), the pulse time of the TMA and H_2O precursors (variable n_4 and n_5, respectively), the gas dwelling time (n_6) as well as the post-growth annealing temperature (n_1) and annealing time (n_2) were chosen to form the set of designed experiment.

III-N MISFETs were fabricated on coupon wafer pieces (~1cm X 1cm). The epitaxial layers consist of a 30 nm AlGaN (Al = 25 %), 1-nm AlN binary barrier and a 3 μm GaN buffer layers grown on a (111) silicon substrate. After the source/drain ohmic contact, a 15-nm-thick Al_2O_3 was deposited by ALD with the designed deposition condition and was annealed in the oxygen atmosphere in an AnnealSys AS-One rapid thermal annealing (RTA) system. Finally, the Ni/Au metal was patterned for the gate formation.

Circular MISFETs under test have the gate width (W_G) of 200 μm, gate-to-source distance (L_{GS}) of 1.5 μm and gate-to-drain distance (L_{GD}) of 1.5 μm. The d.c. current-voltage characteristics were measured in a Keithley 4200-SCS semiconductor parameter analyzer. Three experiment outputs were evaluated to study the effect of each process variable. The threshold voltage (V_{th}) was determined at drain current (I_D) = 1 mA/mm to compare the V_{th} shifting (ΔV_{th}) caused by Al_2O_3 deposition. The gate-to-source leakage current is defined by $Log_{10}(I_{GS})$ at $V_{GS} = V_{th}$ to compare the off-state gate leakage current. The I-V hysteresis is defined as the V_{th} difference ($\Delta V_{hysteresis}$) between the forward and the reverse sweeps.

A two-level experiment, i.e., the "H" and "L" states, was used for each variable designation. To reduce the number of sample required, the designated levels for the

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TMA pulse time (n_5) and the gas dwell time (n_6) in each experiment are generated by $n_5 = n_1 \cdot n_2 \cdot n_3$ and $n_6 = n_2 \cdot n_3 \cdot n_4$. Consequently, a 2^{6-2} fractional factorial design was formed to study six variables using 16 discrete experiments. The detailed process conditions of each sample are listed in Table I.

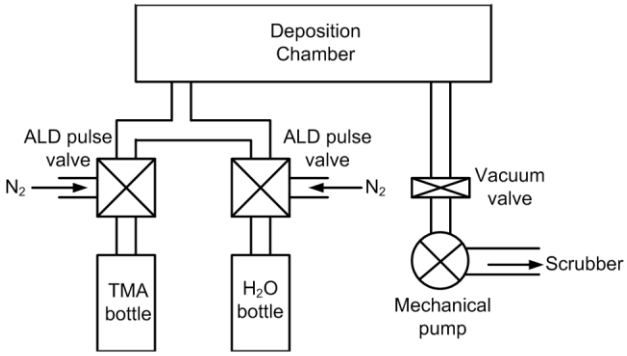

Figure 1 The schematic diagram of the home-made ALD system.

Table I
A list of the assigned levels of each variable in the 2^{6-2} experiment.

Sample Number (j)	experimental variables [n_i]					
	Gas dwell time [n_6]	TMA pulse time [n_5]	H_2O pulse time [n_4]	ALD dep. Temp. [n_3]	Post-dep. Anneal Time [n_2]	Post-dep. Anneal temp. [n_1]
1	L	L	L	L	L	L
2	L	H	L	L	L	H
3	H	H	L	L	H	L
4	H	L	L	L	H	H
5	H	H	L	H	L	L
6	H	L	L	H	L	H
7	L	L	L	H	H	L
8	L	H	L	H	H	H
9	H	L	H	L	L	L
10	H	H	H	L	L	H
11	L	H	H	L	H	L
12	L	L	H	L	H	H
13	L	H	H	H	L	L
14	L	L	H	H	L	H
15	H	L	H	H	H	L
16	H	H	H	H	H	H

In this design of experiment shown in Table I, we can calculate the effect estimates (E_i) of each variables and interactions for each output response using the following equation:

$$E_i = \frac{\sum_j n_{ij} \times y_j}{8}$$

, where n_{ij} =1 at the "H" level or n_{ij} = -1 for the "L" level on the particular variables or interactions. The y_j's are the measured responses. The magnitude of the effect estimate represents the significance of the variable or the interaction. Larger magnitude means the variable or the interaction has more significant impact on the output response of interests. The sign of the effect estimate indicates the variable or interaction having either positive or negative influence on the selected output when the variable or the interaction is at the "H" state.

However, because only 4 variables are fully exploited, the calculated effect estimates (E_i) are confounded by the other variables and interactions. For example, the effect of interaction $n_1 \cdot n_2 \cdot n_3$ *(E123)* is confounded by the effect of n_5 *(E5)* and the interaction of $n_1 \cdot n_4 \cdot n_6$ *(E146)* because n_5 is determined by $n_1 \cdot n_2 \cdot n_3$ and n_6 is determined by $n_2 \cdot n_3 \cdot n_4$. This means that the effect estimate calculated from $n_1 \cdot n_2 \cdot n_3$ is actually a linear combination of *E5, E123* and *E126*. To simplify the result, we assume that high-order interactions are negligible when they are confounded with lower-order interactions since the variables chosen in the experiment have no obvious correlation. Thus, *E5+E123+E126,* for example, can be reduced to *E5* so the effect of n_5 can be determined from the calculation of effect estimate of $n_1 \cdot n_2 \cdot n_3$.

The electrical responses of fabricated MISFETs are of major interest in this study. In particular, three performance parameters were investigated in this experiment. For post-ALD-growth threshold voltage shift (ΔV_{th}), we compared V_{th} with their D-mode HFET counterparts (V_{th} = -7 V) as V_{GS} sweeps from negative voltage to positive ("forward sweep") at V_{DS} = 10 V. The gate leakage current is measured at $V_{GS} = V_{th}$ and $\Delta V_{hysteresis}$ is evaluated at V_{DS} = 10 V.

RESULTS AND ANALYSIS

Five MISFETs were measured on each sample to estimate the average and the variance of each response, as listed in Table II. The ΔV_{th} varies from -3.5V to -15V, suggesting different positive charge density may exist in Al_2O_3 layer grown by different conditions. The GS diode leakage also varies between < 1 pA to 10 μA. The variation in the I-V hysteresis also suggested different $Al(OH)_x$ concentration in Al_2O_3 layer [3]. To determine which variable and interaction are the statistically important, the calculated effect estimates were plotted against the accumulative probability. In these plots, the effect estimate values arising from the measurement noise follow the normal distribution and form a straight line near the origin of the plot while the most important variables and interactions are located at the corner.

Table II
The average values and variance of measured responses.

Sample Number (i)	Measurement Data Summary					
	ΔV_{th} (I_D=1mA/mm)		$\Delta V_{hysteresis}$ (between forward and reverse sweep)		Log_{10} (I_{GS}) (at $V_{GS}=V_{th}$)	
	Avg.	Var.	Avg.	Var.	Avg.	Var.
1	-13.52	0.44	1.57	0.003	-7.03	1.78
2	-14.52	0.04	0.33	0.013	-3.96	0.03
3	-15.02	0.21	0.6	0.13	-6.37	0.65
4	-6.22	0.54	1.03	0.003	-13.1	0.02
5	-13.72	0.6	0.07	0.003	-5.17	1.27
6	-8.42	0.02	0.6	0.01	-12.3	0.01
7	-6.52	0.14	0.07	0.006	-7.4	2.47
8	-7.22	0.82	0.67	0.013	-13	0.02
9	-13.02	1.01	0.13	0.003	-4.4	0.01
10	-13.62	1.39	0.2	0.03	-6.55	0.05
11	-9.22	0.02	0.1	0.001	-5.8	1.86
12	-5.82	0.07	0.83	0.003	-12.6	0.01
13	-12.02	0.16	0.13	0.023	-6.17	0.38
14	-8.12	0.14	0.1	0.01	-6.53	1.12
15	-15.12	0.5	0.37	0.003	-5.89	0.16
16	-3.52	0.09	0.3	0.001	-6.68	0.11

In Figure 2, the plot shows that the annealing conditions (*E1* and *E2*) and ALD growth temperature (*E3*) have strong positive effect on V_{th}. The TMA pulse time (*E5*) and gas dwell time (*E6*) may slightly reduce V_{th}. However, *E5* and *E6* fall into the variance of response so they may not be statistically significant. This result suggests higher annealing temperature, longer annealing time and higher deposition temperature may be preferred for less V_{th} shift (more positive V_{th}) on MISFETs.

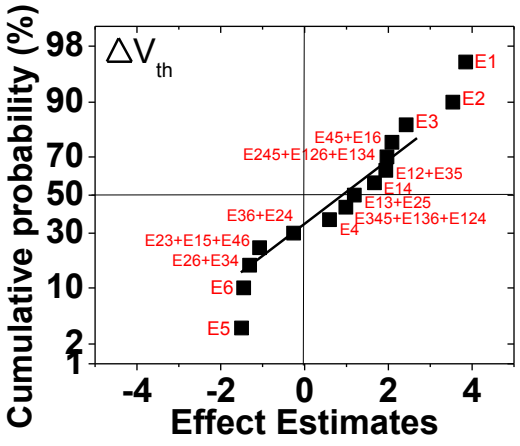

Figure 2 The effect estimates for V_{th} of MISFETs

In terms of the gate leakage reduction, higher temperature (*E1*), longer annealing time (*E2*) and their interaction (*E12*) shows a trend of reducing the gate leakage while longer precursor pulse time (*E5* and *E4*) may increase the leakage current, as shown in Figure 3. The statistically significant interactions are also related to *E245+E126+E134*. When the V_{th} effect is also taken into consideration, shorter TMA pulse width (negative *E5*), longer H_2O pulses (negative *E245* and *E134*) and shorter gas dwell time (negative *E126*) could lead to reduced gate leakage current and less threshold voltage shift.

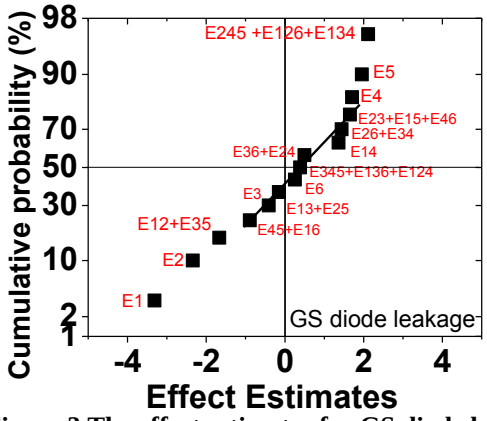

Figure 3 The effect estimates for GS diode leakage current ($Log_{10}(I_{GS})$) at $V_{GS}=V_{th}$.

We also determined that higher ALD growth temperature (*E3*) and longer precursor pulse time (*E4* and *E5*) may help reduce the *I-V* hysteresis of MISFETs, as shown in Figure 4. Assuming these variables also contribute to major interactions, statistically significant interactions are *E35+E12*, *E34+E26* and *E134+E126+E245*, respectively, which have opposite effect in the increase of the I-V hysteresis. This implied a trade-off growth condition design would exist for the precursor pulse time and the ALD deposition temperature. Combined with the analysis of V_{th} control and the gate leakage, we conclude that shorter TMA pulse width and longer H_2O pulse width are preferred for smaller post-ALD growth V_{th} shift, low gate leakage current and lower I-V hysteresis.

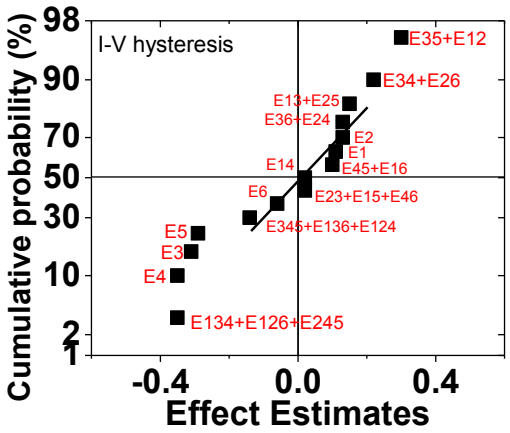

Figure 4 The effect estimates for measured I-V hysteresis ($\Delta V_{hysteresis}$)

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Based on this analysis, an optimal ALD deposition and annealing condition are determined with high annealing temperature, longer annealing time, higher ALD deposition temperature, longer H_2O pulses, shorter TMA pulses and shorter gas dwell time. Using this combination of parameters, AlGaN/GaN circular MISFETs were fabricated on a coupon pieces of the same wafer under this study. In Figure 5, the measured transfer curves show V_{th} of -12 V, which corresponds to ΔV_{th} < 5 V. I-V hysteresis is < 0.5 V at V_{DS} = 10 V when the gate voltage sweeps between -17 V and 0V. The off-state drain leakage is < 1 pA/mm at V_{DS} = 10 V and a gate-to-source leakage current of < 1 pA/mm was measured at V_{GS} = -12 V (the inset of Figure 5 (a).) The family curves show I_{DSS} > 400 mA/mm with R_{DSon} of 15 Ω-mm at V_{GS} = 0V and V_{DS} = 1V. The drain-to-source breakdown voltage (BV_{ds}) also shows a value of greater than 170 V, corresponding to lateral breakdown field of 1.1 MV/cm (the inset of Figure 5 (b).) The results confirm the validity of the current ALD optimization study.

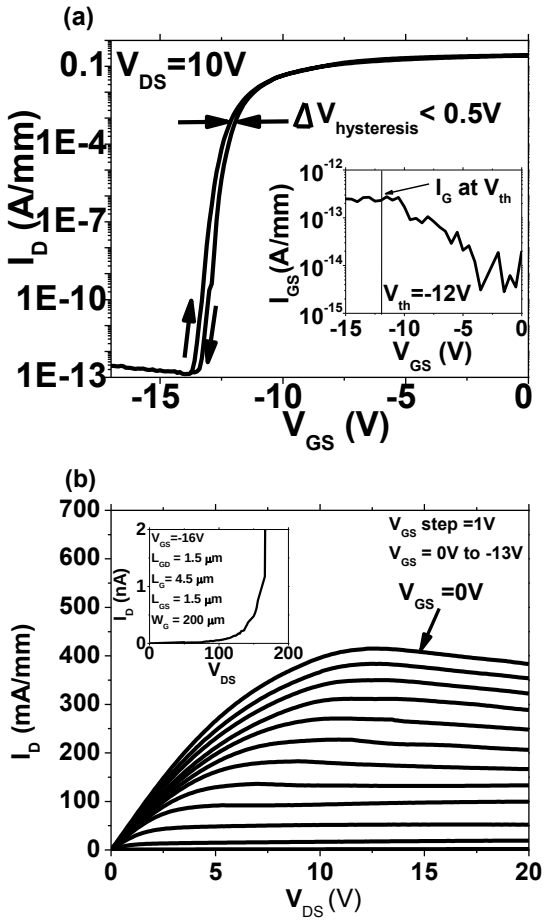

Figure 5 I-V characteristics of circular MISFET with W_G = 200 µm and L_{GD} = L_{GS} = 1.5 µm (a)Forward and reverse sweep of transfer curves (b) I_D-V_{DS} family curves and breakdown voltage (inset)

CONCLUSIONS

In summary, we have studied Al_2O_3 processing conditions on AlGaN/GaN MISFETs. A 2^{6-2} two-level fractional factorial design of experiments helps determine a possibly optimal processing recipe to achieve good V_{th} control, low gate leakage, low I-V hysteresis and high breakdown voltage characteristics in GaN-based MISFETs. Fabricated MISFET with L_{GD} = 1.5µm shows V_{th} of -12 V, I-V hysteresis < 0.5 V, and gate leakage < 1pA/mm. The drain-to-source breakdown voltage (BV_{ds}) of greater than 170 V is achieved, corresponding to lateral breakdown field of 1.1 MV/cm.

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ACRONYMS

MISFET: Metal-Insulator-Semiconductor Field-Effect Transistor
HEMT: High electron mobility transistor
ALD: Atomic Layer Deposition
TMA: Trimethylaluminum
RTA: Rapid thermal annealing
GS diode: Gate-to-source diode