Yield Learning of a GaAs-Based High-Throw-Count Switch for Handset Applications

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Abstract

This paper will discuss the path to yield improvement of a high-throw-count handset switch in the pre-production release phase. This work was necessitated by lower than expected initial yields found to be due to excessive off state current of the switch die. Failure analysis was performed leading to the generation of a die sort test plan specific to the switch. After tracing the origin of the failure mode back to the fab, we started a systematic approach to removing fab defects from the process. Defect reduction leading to improved yields was accomplished by employing Automated Optical Inspection intimately with process auditing and line partitioning at targeted steps in the fabrication process.

INTRODUCTION

In 2011, TriQuint introduced a new dual-band transmit module to the handset market containing a GaAs-based high-throw-count switch on a process named TQP25 [1, 2]. Initial pre-production yields were below expectations, and the switch was found to be the cause. Stringent application-specific DC die sort test requirements, increased process complexity, and switch design topology employing a high gate density were all factors in the depressed yield. Failure analysis showed that for the first time at TriQuint, a high-volume RF product was yield-limited due to process defects, rather than parametric variation. Reducing defects to enable high yield and reliability has long been critical for Silicon manufacturing, but for GaAs manufacturing parametric failures are often on top of the yield Pareto.

SWITCH TEST DEVELOPMENT

A handset module must perform to very strict electrical specifications for use in a typical application, and the switch function is an integral part of this. The switch must comply with exacting intermodulation distortion (IMD) and harmonic (H2/3) levels. Since IMD and harmonics are costly and difficult to test at the production level, the switch must be "known good" going into module assembly. This requirement puts the onus on screening at the DC or RF die sort level. Since RF die sort is also costly, TriQuint focused on screening at the DC die sort step.

Early in the release of a typical high-throw switch (here greater than 6 arms), some sample devices were found to fail IMD3 and H3 in specific paths, in the Transmit path for example. Interestingly, the neighboring paths were normal. The failures were not marginal; typically the values were 20 dBm out of population for IMD3. At the switch level, IMD3 and H3 performance is dictated by both on- and off-arm device performance. Since the on-arm performance is typically solid, the off-arm behavior of all the other paths was quickly suspected.

An off device in a typical switch topology needs to be completely off and have a very predictable performance across voltage. To aid in switch linearity, resistors are placed between the Drain and Source, in parallel with the FET channel. The switch design stacks a number of FETs in series for harmonic performance, which makes measuring this series of Drain-Source resistors easy when probing between the Antenna and Vdd ports of the switch. Probing these resistors for the off devices is what led to the realization that something was indeed amiss with the off-arms in the failing die as the total resistance was abnormal.

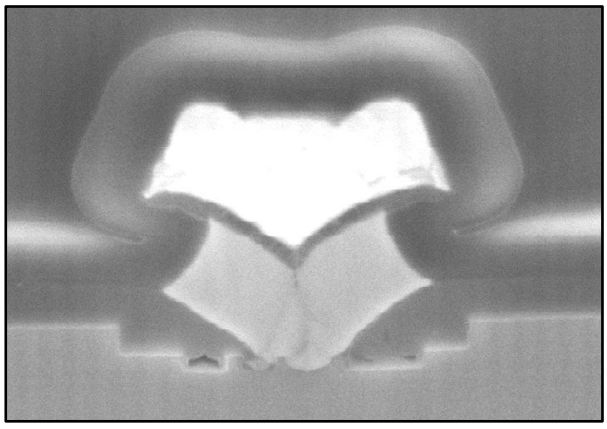

FIGURE 1: Focused Ion-Beam cross-section of a DFET identified as causing off-state leakage. Incomplete etching of the narrow recess at the bottom of the gate is observed.

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Failure analysis was able to identify a number of die that had lower and variable resistance of the off-arms when comparing against a known good die. Light emission analysis was employed to identify the source of the low resistance path, which was found to be caused by numerous point sites within the switch arm. These sites were then cross-sectioned using a Focused Ion-Beam (FIB), and the results are shown in Figure 1. The cross-section in this Figure shows that a small portion of the FET in the switch arm is not being completely controlled by the gate; there is essentially an off-state leakage path. This leakage path shorted around the channel resistor for that FET and is what caused the overall off resistance to drop.

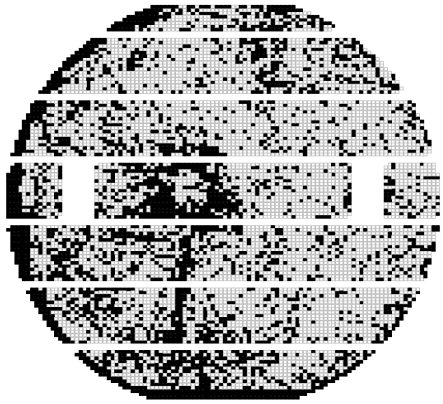

FIGURE 2: DC die sort wafer map of showing die failing for excessive off current (black).

Driven by the analysis of the fallout, a new DC die sort test was developed, which was able to measure the current through the Drain-Source resistors of the switch arms when turned off. Since each arm may have a different set of resistor values, post processing was necessary to compare the measured value versus an expected value based upon each switch's design. The post processing also allowed some normalization to account for the sheet resistance roll off across the wafer of the thin-film resistors. The leakage current through a bad FET removed that specific channel resistor out of the total chain, so the data from this test, named Roff, tended to fall into almost quantized distributions, and it also made it easy to see how many total FETs were failing in each measured path. In addition to checking the health of the switch FETs, the Roff test also tested the functionality of the resistor chains on die for abnormal resistor processing, which would also cause switch linearity failures.

Once the Roff test was implemented and data were available from numerous wafers, distinct patterns became apparent. Figure 2 shows a typical early gross failure pattern of failing die with excessive off current. Additional effort was made to validate the same failure modes across different failure patterns on the wafer maps, and the majority of the cases supported incomplete FET formation.

DEFECT REDUCTION EFFORTS

The combination of the FIB cross-sections showing incomplete FET creation due to an apparent etch blockage along with the die sort maps showing a random background pattern to the Roff failures facilitated the connection between processing defects and Roff yield loss. TriQuint had encountered yield loss caused by defects before [3], so a similar cross-functional team was formed to understand and eliminate the defects.

The FIB cross-sections and SEM images of identified defects clearly showed that steps before the gate metal was deposited were critical, so this limited the number of process steps to consider. In spite of this however, there are numerous different dielectric and substrate etches that occur prior to metallization, and blockage of any of these etches could cause elevated FET off current, so it was necessary to investigate all operations from the beginning of the process up to gate metallization. Line partitioning, or focusing on specific groups of process sequences, was the main method selected for determining the sources of defects. The goal was to find an operation or set of operations that were creating the majority of the defects.

As early Automated Optical Inspection (AOI) data were compared to DC die sort parametric data, in-line defect patterns and locations on wafer discovered at a given process step matched the die sort parametric yield loss locations quite well, as shown in Figure 3. Thus, strong correlations between the sampled process step (AOI before an etch for example) and Roff fallout patterns were established. This is demonstrated in Figure 4 where defect densities measured by AOI at a specific processing step are plotted against Roff yield variation from what was expected.

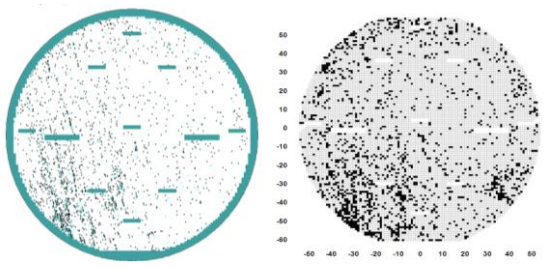

FIGURE 3: AOI defect maps on the left showed similar defect locations to yield loss patterns in die sort maps on the right.

This discovery eliminated ~ 1/3 of the target operations and allowed us to focus our efforts on a smaller set of tools and processes.

There was another benefit of this discovery. Until this time, Roff yield loss on wafer maps was the primary source of data to learn about the yield loss, but that happened very late in the process flow. There was now proof that defect maps would mimic parametric maps. Now, AOI defects maps produced early in the process flow could be used to predict final yield improvements and to get quick feedback about process splits which shortened the learning process by weeks.

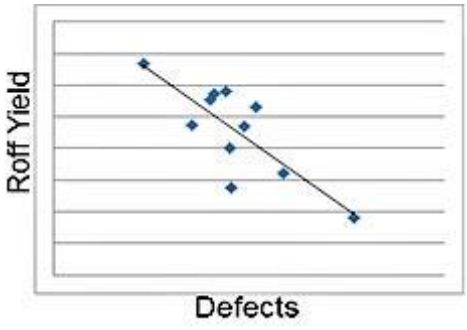

FIGURE 4: AOI defect levels showed good correlation with Roff test yields.

USING ESTABLISHED TECHNOLOGIES

A unique challenge that newly released processes present is low initial wafer volume, which does not drive large data sets. Data trends are important with random defects, but small sample sizes make it difficult to distinguish the signal from the noise. Two primary techniques to compensate for the low volumes on the new process were used.

First, the TQP25 technology had been cleverly developed to share many operations with an existing pHEMT process flow, in fact about 75% of the processing steps were the same for the targeted operations. This similarity reduced costs and complexity in the factory in addition to cutting development time. The existing pHEMT route was running high volumes of a particular product which was used a proxy for the new process route through various line partitions.

Second, a review of past defect reduction efforts on completely different processes was conducted. It was known that sinks could cause defect transfer from the backs of one wafer to the front of an adjacent wafer during rinses using spray bars. Further learning about this defect mode showed us that defect transfer happened even without water spray and that particular sinks were more susceptible to transferring defects than others. The proxy pHEMT process route was used to confirm that a suspect sink produced similar defects as witnessed in the past. Trend charts were then analyzed by tool at a suspect operation. The problem tool was highlighted, and defect wafer maps were compared from problem lots showing similar patterns to what had been seen previously. The suspect sink was shut down for processing vulnerable layers.

The investigation in the back to front defect transfer mechanism continued by investigating wafer orientation in the cassette during processing. It was discovered that significant changes in orientation, would further reduce the chances of defect transfer. New process tools were purchased and introduced that automated the orientation changes which ensured defect free handling in the fab.

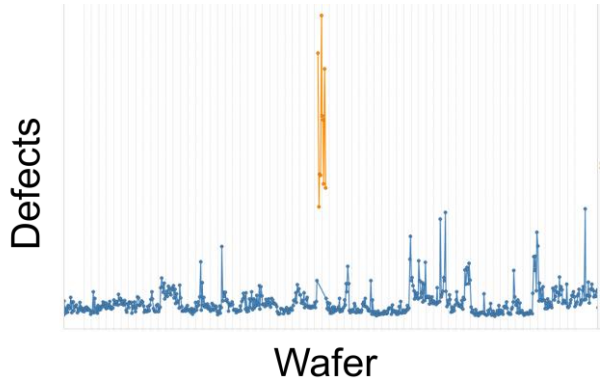

FIGURE 5: Wafers from one epi shipment had much higher defects than other cleaner shipments

Another benefit of the high volume process flow was to highlight the differences that epi suppliers can have on defect levels. Figure 5 shows the differences that certain epi shipments can have on defect levels. For a process and circuit topology that is highly dependent on low defect levels to achieve high yields, improvements in epi defects can have a large benefit. TriQuint used information from data presented in this paper to work with our epi suppliers on defect reduction efforts.

WAFER MAP OVERLAY

As the wafer volume began to ramp to production-like levels, a wafer map overlay technique was used to help determine where defects originated. This technique is where defect wafer maps of the same wafer from different inspection operations are overlaid and viewed electronically. Software is used to determine adder defects using a 50 um correlation radius before and after a specific step. One limitation of this technique was known, where variations in the contrast on the wafer could cause the tool to miss defects at one inspection step that it had caught at prior steps.

As defect wafer maps at all of the inspection operations were studied, a common streaking pattern was observed which is shown in the AOI map in Figure 3. Overlay of the wafer maps showed that this pattern was present at the first

inspection operation. The line was partitioned through the operations at the very beginning of the process, to find when the streak pattern first appeared. By comparing AOI inspection results of bare incoming wafers before and after specific portioned steps, it was discovered that a preparatory sink process was the cause. In order to determine the make-up and composition of the particles, Knights Tracking software installed on a FIB was used to import a defect wafer map and drive to specific defects for EDX analysis. This analysis determined that the defects were GaAs particles.

Meanwhile, particle analysis of the suspect sink was showing very few particles being added to test wafers. It was decided that the streak defects were coming in on the raw wafer in clusters. The sink process was then loosening the cluster of GaAs particles and re-distributing them across the wafer.

Multiple experiments were run to remove the particles before they could be re-distributed in the sink, and a suitable candidate was found. Analysis showed that the process of record resulted in an increase of over 1000 particles through re-distribution while the new cleaning process had a decrease of almost 500 particles and no streaking pattern, shown in Figure 6. Follow up experiments demonstrated that the higher the number of incoming particles, the greater the effectiveness of the new clean, confirming suspicions of the particles' origin.

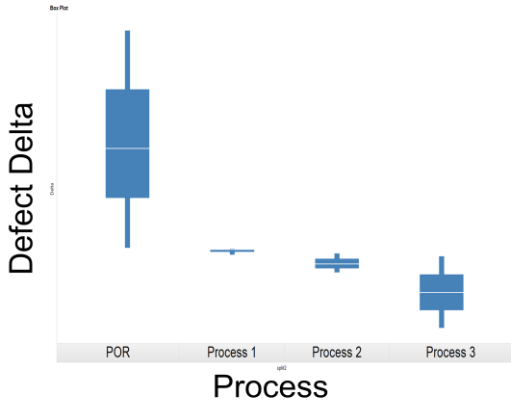

FIGURE 6: Cleaning processes were found to remove incoming wafer defects.

OBSERVATION OF PATTERNS

Wafer map observation is a key tool for the defect engineer to use to find defect sources. In the case of TQP25, a unique defect signature was found which highlighted the need to follow proper handling procedures. Both AOI defect wafer maps and parametric yield maps had shown defect clusters near the edges of wafers. Often they were seen on one or more wafers in a lot, but never on the whole lot. Overlay of defect wafermaps showed that the adders happened in between two inspection operations, thus all of the operation steps in between were scrutinized. Process knowledge as well as the unique signature of the defects led us to suspect a SEM operation where single wafers were used for a gate length measurement. Investigation showed that the wafer with the defect signature was indeed the wafer being pulled for SEM measurement and that the same operator was processing the lot each time. Wafer handling errors were identified, and the operator was immediately retrained which eliminated the yield loss.

Another observation was that defects and yield loss happened occasionally in wide arcs along the edges of random wafers. Inspection of the defective areas of the wafers revealed that a known effect was reducing yield for the first time. The effect was created by gas-phase nucleation during the oxide deposition process. TriQuint had been aware of this effect in the oxide layer for years, but it had never affected yield. It was intermittent and mostly confined to low volume flows, so work was focused on higher priority yield issues. On TQP25, this defect did decrease yield by shifting the value of thin-film resistors used in the Roff test as mentioned previously, so its elimination became a high priority. PECVD process experts gave advice on process changes which had a beneficial impact. TriQuint colleagues in Texas also provided valuable information whereby an excursion of this oxide effect was fixed through a hardware change on their tool. In Oregon, the properly functioning existing hardware was replaced to test if new hardware improved the situation. The combination of both improvements resulted in elimination of the effect and yield improvement of 10-15% on the random wafers it affected.

CONCLUSION

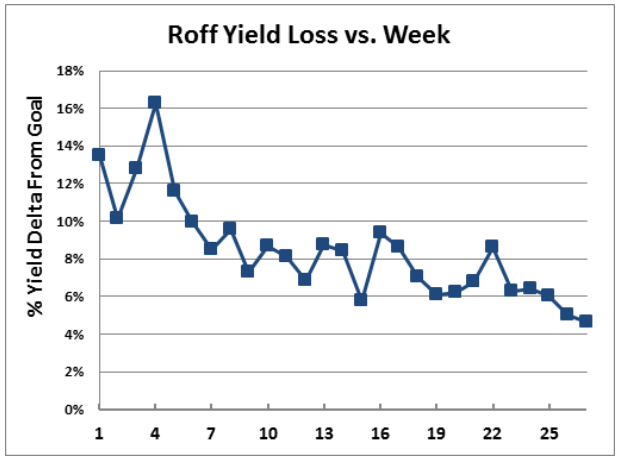

FIGURE 7: Yield was continuously improved with a focus on defect reduction

Low pre-production yields on a handset switch die were found through specific die sort tests. Failure analysis determined the yield fallout was due to excessive off currents driven by incomplete formation of DFETs. A broad study of different failures showed that defects were found to impact yield significantly on an important new product. A cross-functional team was formed to reduce defect levels. They used analysis techniques to determine the sources of some major contributors to yield loss. TriQuint used line partitioning and defect source analysis to find key operations where defects originated. AOI was used to verify experiments and drive process improvements. Pattern observation was also an aid to defect source discovery. Various analysis techniques combined with effective teamwork allowed us to drive yields to very close to our expectations for this new product, see Figure 7.

A final benefit that this project produced was the ability to monitor process health by looking at defect trends while wafers are processing instead of having to wait for parametric testing. TriQuint can now react to tool and process excursions more quickly by performing inline inspections on randomly chosen lots. Line partitioning techniques not only helped to make the process better but are now used to keep the process healthy and to keep yields high.

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ACRONYMS

pHEMT: pseudomorphic high-electron mobility transistor
DFET: Depletion-mode field effect transistor
AOI: Automated Optical Inspection
FIB: Focused Ion Beam
IMD: Intermodulation Distortion