

# GaN MOSHEMT using Sputtered-Gate-SiO<sub>2</sub> and Post-Annealing Treatment

Liang Pang<sup>1</sup>, Yaguang Lian<sup>1</sup>, Dong-Seok Kim<sup>2</sup>, Jung-Hee Lee<sup>2</sup>, and Kyekyoon Kim<sup>1</sup>

<sup>1</sup>Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, IL 61801

<sup>2</sup>School of Electrical Engineering and Computer Science, Kyungpook National University, Korea, 702-701

E-mail address: [kevinkim@ad.uiuc.edu](mailto:kevinkim@ad.uiuc.edu)

Tel: (217)-333-7162

**Keywords:** GaN MOSHEMT, Sputtered-SiO<sub>2</sub>, Post-annealing, Breakdown voltage

## Abstract

By using RF magnetron sputtering with oxygen compensation in the gas environment, high-quality SiO<sub>2</sub>-on-GaN with breakdown field of 9.6 MV/cm was achieved. A post-annealing treatment was further developed to remove the sputtering-induced epilayer damage, which not only recovered, but improved the electron concentration and mobility of the 2-D electron gas by 21.7% and 5.5%, respectively. High-performance SiO<sub>2</sub>/AlGaIn/GaN MOSHEMT was thus fabricated, which exhibited a maximum drain current of 594 mA/mm and a breakdown voltage of 205 V at the gate-drain distance of 2 μm. The breakdown voltage performance is among the best of GaN-based HEMTs or MOSHEMTs reported to date.

## INTRODUCTION

Although GaN-based HEMTs have attracted considerable attention for high-power, high-speed and high-temperature application, relatively large gate leakage through the metal/GaN contact remains to be a serious problem [1]. To find a solution, significant progress has been made on MOSHEMTs, where the gate-oxide, like SiO<sub>2</sub>, is formed via various techniques like PECVD, electron-beam evaporation or ALD [2-4]. RF magnetron sputtering has been proved to be able to deposit SiO<sub>2</sub> on GaN with quality better than the above-mentioned techniques [5], since the energetic particle impingement can make the growing film more condensed, therefore enhancing the oxide breakdown field. However, due to the difficulty to prevent bombardment damage to the epilayer that degrades the 2DEG properties, there are very few reports on the successful fabrication of MOSHEMT employing sputtered gate-SiO<sub>2</sub>.

In this study, we first optimize the sputtering condition to produce high-quality SiO<sub>2</sub> on GaN, and then propose a post-annealing treatment to remove the sputtering-induced surface damage. As a result, sputtered-SiO<sub>2</sub> MOSHEMT with high current and breakdown voltage characteristics is demonstrated.

## EXPERIMENTAL

Firstly, Al/SiO<sub>2</sub>/n<sup>+</sup>-GaN ( $n = 1.4 \times 10^{19} \text{ cm}^{-3}$ ) MOS-capacitors were fabricated to examine  $V_{br}$  of the SiO<sub>2</sub> film under different deposition conditions. The sputtering was carried out at room temperature with a constant power of 160 W. Argon and oxygen (with different ratios) were used as the sputtering gas. Secondly, Hall-effect measurements were conducted to investigate the impact of sputtering damage on the 2DEG properties, and the efficacy of post-annealing treatment for damage recovery was systematically analyzed. Finally, SiO<sub>2</sub>/AlGaIn/GaN MOSHEMTs were fabricated as follows. After device isolation and recessed source/drain etching, 10-nm SiO<sub>2</sub> was sputtered at the optimized condition on the template. Ti/Al/Ti/Au were then deposited by electron-beam evaporation as the Ohmic contacts, followed by post-annealing in N<sub>2</sub> ambient. Deposition of gate metals (Ni/Au) completed the fabrication process.

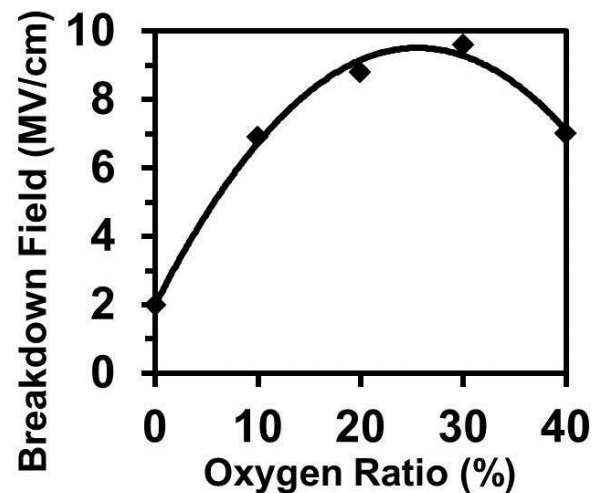


Fig. 1. Breakdown field of the sputtered-SiO<sub>2</sub> films on n-GaN as a function of oxygen ratio in the sputtering gas.

## RESULTS AND DISCUSSIONS

$V_{br}$  of the SiO<sub>2</sub> film strongly depends on different sputtering conditions, like the oxygen ratio in the sputtering gas. As shown in Fig. 1, continuous improvement in  $V_{br}$  was found when increasing the oxygen ratio up to 30%. By introducing oxygen atoms into the film, the oxygen vacancies normally occurred during sputtering were compensated, therefore eliminating the defects and enhancing the film quality. Beyond 30% oxygen ratio,  $V_{br}$  started to decrease, which is attributable to the reduction of energy input into the film due to the smaller atomic mass of O than Ar, thus reducing the film density. The largest  $V_{br}$  of 9.6 MV/cm is higher than that of the SiO<sub>2</sub> films deposited on GaN by other techniques like PECVD, photo-CVD, and electron-beam evaporation [6-8].

Table 1. Values of the electron concentration ( $n_s$ ) and mobility ( $\mu$ ) under different annealing temperatures and durations.

Experimental conditions	Electron mobility (cm <sup>2</sup> /V·S)	Sheet concentration ( $\times 10^{13}$ cm <sup>-2</sup> )
Epilayer	1060	1.08
RTA (0 °C, 0 s)	330	0.81
RTA (800 °C, 20 s)	644	0.98
RTA (900 °C, 20 s)	1118	1.32
RTA (1000 °C, 20 s)	1077	1.30
RTA (900 °C, 10 s)	941	0.99
RTA (900 °C, 30 s)	1116	1.31
RTA (900 °C, 60 s)	974	1.25

After optimizing the sputtered-SiO<sub>2</sub> quality, the impact of sputtering damage on the 2DEG properties was investigated. Hall-effect measurements showed that after 10-nm SiO<sub>2</sub> was sputtered on the AlGaIn surface with 30% oxygen mixing,  $n_s$  and  $\mu$  decreased by 25% and 69% respectively, which was resulted from the sputtered-induced interface states. In order to improve the interface quality, a post-annealing treatment was developed. Table 1 shows the values of  $n_s$  and  $\mu$  under different annealing temperatures or durations. It can be seen that performing the post-annealing at 900 °C for 20 s is able to fully restore the epilayer crystallinity and interface quality. The additional improvement in both  $n_s$  (21.7%) and  $\mu$  (5.5%) is due to the chemical passivation of the exposed epilayer surface dangling bonds by the SiO<sub>2</sub> film. Further increasing the annealing temperature or time resulted in reduction of  $n_s$  and  $\mu$  again, owing to the defect generation by AlGaIn/GaN film dissociation at the elevated temperature, which degraded the epilayer crystallinity and channel interface morphology. Furthermore, it was found that

the optimized post-annealing condition coincides with that of the GaN-based Ohmic metal annealing for Ti/Al contact scheme, which is generally performed at 850~900 °C for 20~30 s. Therefore, these two steps can be combined to save the thermal cost and simplify the fabrication process. As a result, our process may be considered to have the lowest thermal energy requirement to realize MOSHEMT among all the dielectric deposition techniques, which is beneficial for commercial applications.

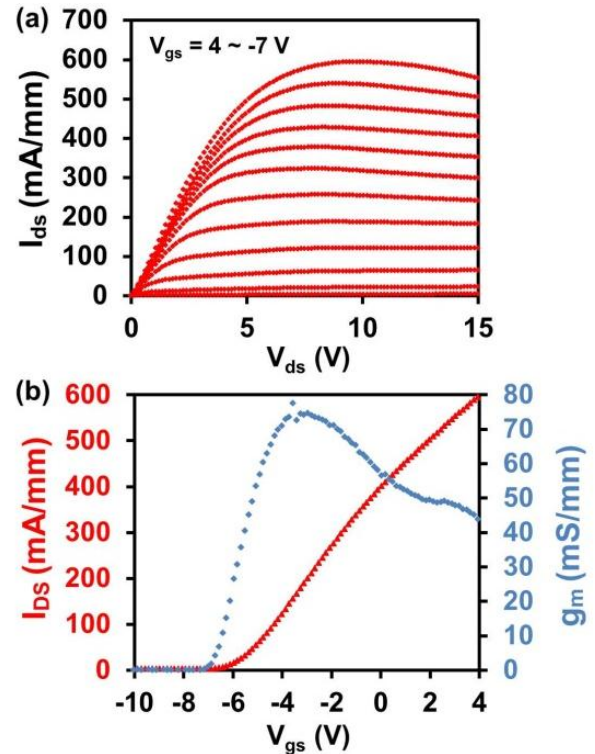


Fig. 2. (a)  $I_d$ - $V_d$  and (b) transfer characteristics of the AlGaIn/GaN MOSHEMT with 10-nm sputtered-SiO<sub>2</sub>.

Based on the optimized sputtering and post-annealing conditions, sputtered-SiO<sub>2</sub>/AlGaIn/GaN MOSHEMT was fabricated. For the device dimension, the gate length, width, source-to-drain and gate-to-drain distances were designed to be 2  $\mu$ m, 100  $\mu$ m, 6  $\mu$ m, and 2  $\mu$ m, respectively. During the process, RTA was carried out at 900 °C for 20 s for both sputtering damage elimination and Ohmic contact formation. For the characterization, the gate leakage current of the MOSHEMT was first compared with the conventional HEMT of the same dimension. It was found that at the reversed gate bias of -30 V, more than four orders of magnitude lower leakage current was achieved by using the MOSHEMT. The  $I_d$ - $V_d$  and transfer characteristics were then investigated (Fig. 2). The peak drain

current and the maximum transconductance were 594 mA/mm and 74.5 mS/mm, respectively. The three-terminal off-state breakdown voltage was measured by a curve tracer and was 205 V. A comprehensive comparison of the breakdown voltages per unit gate-drain distance, obtained from various publications [8-15], is presented in Fig. 3. The dielectric thickness is also taking into consideration, since a direct comparison using MOSHEMTs with the same dielectric thickness is difficult. The breakdown voltage performance of our device is, if not better than, on-par with other GaN-based MOSHEMTs reported to date.

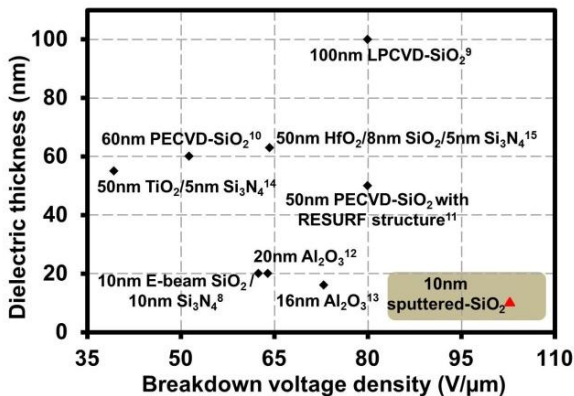


Fig. 3. Comparison of breakdown voltage density of MOSHEMTs achieved by different groups.

## CONCLUSIONS

Using room temperature RF magnetron sputtering with 30% oxygen mixing, highly condensed SiO<sub>2</sub> has been demonstrated to be a suitable gate insulator for GaN-based MOSHEMTs. Further adopting the post-annealing treatment during Ohmic contact formation effectively removed the sputtering-induced epilayer damage, resulting in the MOSHEMT with high saturation current and breakdown voltage.

## REFERENCES

- [1] I. Daumiller, *et al.*, IEEE Electron Device Lett. **20**, 448 (1999).
- [2] M. A. Khan, *et al.*, Appl. Phys. Lett. **77**, 1339 (2000).
- [3] S. Arulkumaran, *et al.*, J. J. Appl. Phys. **44**, L812 (2005).
- [4] Z. H. Liu, *et al.*, IEEE Electron Device Lett. **31**, 803 (2010).
- [5] L. Pang, *et al.*, J. Phys. D, Appl. Phys. **45**, 045105 (2012).
- [6] H. Ueda, *et al.*, J. J. Appl. Phys. **48**, 126001-1 (2009).
- [7] Y. Z. Chiou, *et al.*, IEEE T. Electron Device **50**, 1748 (2003).
- [8] N. Q. Zhang, Ph.D dissertation, Univ. CA, Santa Barbara, 2002.
- [9] K. Matocha, *et al.*, IEEE T. Electron Device **52**, 6 (2005).
- [10] H. Kambayashi, *et al.*, Solid-State Electron. **54**, 660 (2010).
- [11] Y. Niiyama, *et al.*, Furukawa Rev. **36**, 1 (2009).
- [12] M. Kanamura, *et al.*, IEEE Electron Device Lett. **31**, 189 (2010).
- [13] P. D. Ye, *et al.*, Appl. Phys. Lett. **86**, 063501 (2005).

- [14] S. Yagi, *et al.*, J. J. Appl. Phys. **46**, 2309 (2007).
- [15] S. Yagi, *et al.*, Phys. Status Solidi c **4**, 2682 (2007).

## ACRONYMS

- HEMT: high electron mobility transistor  
MOS: metal-oxide-semiconductor  
2DEG: 2-dimensional electron gas  
PECVD: plasma-enhanced chemical vapor deposition  
ALD: atomic layer deposition  
V<sub>br</sub>: breakdown voltage/field  
n<sub>s</sub>: electron concentration  
μ: electron mobility  
RTA: rapid thermal annealing

