

Process-Reliability Relationships in GaN and GaAs Field Effect Transistors and HFETs

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Abstract

Although accelerated life testing of low noise and power GaAs MESFETs under d.c. bias and RF operation has been conducted, some failure mechanisms remain to be of concern. We will address these concerns and will report on failure models of AlGaAs/GaAs HFETs. The set of reliability physics models then will form the starting point for development of physics based failure models for GaN HFETs devices. Processes in effect in GaN, but not in GaAs, owing to higher fields and much larger field, temperature, and strain coupling are included.

FAILURE MODES AND MECHANISMS OF AlGaAs/GaAs HFETs

The AlGaAs/GaAs HFET degradation mechanisms, beyond those for GaAs MESFETs, include deep levels in the barrier and changes in the 2DEG concentration. The I-V collapse in the dark, and persistent photo-conductivity are more related to the material quality than to the long-term device stability. The decrease in 2DEG density is due to carrier deconfinement, enhanced by field-aided impurity diffusion at the heterointerface (would also occur in GaN HFETs). The defects, present or created by high field (temperature, strain) followed by hot electron capture, would reduce the available carriers. These anomalies also cause high levels of LF noise. Similar effects must undoubtedly take place in the GaN system. Extensive analyses coupled with test heterostructures have been undertaken to uncover the nature of these anomalies for the failure model development. Electromigration plays an important role in GaAs HFETs since GaAs, [1,2] being a binary compound, may have a wide variety of surface conditions (various native oxides and their clusters, surface states etc.). Further, electromigration is influenced by conductor-line material parameters and inhomogeneities, as well as structural features of the conductor layout, etc.

GaN FET PHYSICS OF FAILURE/DEGRADATION

The degradation mechanisms germane to GaN, in addition to those present in GaAs, are primarily related to surface traps,

metal semiconductor and inter-metal diffusion, compound formation, interface and bulk defect states. However, local high fields (\gg GaAs) coupled with strain and temperature as well as the increased hot phonon generation will alter the key GaN HFET degradation mechanisms. Clearly, the GaAs model has been a starting point which has been followed with its expansion to incorporate the GaN specific mechanisms. A variety of "trap" related device effects are reported which include transconductance frequency dispersion, current collapse, light sensitivity, gate- and drain-lag transients, and restricted microwave power output. The activity directed toward characterizing these effects parallels similar developments in the GaAs-based technology.

Electron capture-emission by surface and bulk traps affects the 2DEG density resulting in current collapse, and transconductance dispersion. Because the associated characteristic time is $\sim 1\text{ns} < \tau < 1\text{ s}$, the trapping limits device performance even at relatively low frequencies. In addition, the thermally activated traps contribute significantly to LF noise. Understanding the origin of the traps in GaN-based transistors, their physical and energy location, and the physical mechanisms involved in the trapping is critical for not just the optimization of device performance, but for reliability modeling and reliability optimization for the GaN HFETs. Degradation caused by surface states and preexisting bulk and interface states are reversible. However, when new defects begin to be created and their density cascades due to the combined effects of high field, heat and strain, the resulting device degradation becomes catastrophic.

a Bulk buffer traps

Bulk traps in early GaN MESFETs and HFETs have been investigated. The fitted photoionization thresholds located the two dominant defects at ~ 1.80 and 2.85 eV below the conduction band edge, and after the 0.55 eV and 0.2 eV Franck-Condon correction, respectively. The DX centers plausibly associated with O have been observed in AlGaIn may also be present. The enhancement of the optically induced drain-current recovery for photon energies at or above the band gap, E_g , of GaN has been measured and in

contrast, no such increase for photon energies above E_g of AlGaN has been observed, hence, placing the traps to be within GaN buffer layer. However, it is obvious that further investigations are necessary in order to attain a complete understanding. For instance, one trap appears to be correlated with MOCVD growth pressure since the trap density increases at lower pressures [3,4].

b. Surface traps

A strong correlation of gate lag with the surface treatment suggests that at least some trapping centers, besides the bulk GaN and AlGaN traps, are located at or near the surface. Surface trapping can be identified by measuring gate lag for devices with different surfaces achieved by chemical treatment or dielectric passivation. The temporal character of charge emission from these traps is typically a stretched exponent with a characteristic time in the range of seconds. Kelvin probe microscopy showed that electrons migrate 0.5–1 μm along the surface away from the gate. An area of particular concern is the limiting effect of electronic traps on RF performance. Electrostatic force and Kelvin probe microscopes can measure both local surface charge and potential with high spatial resolution. Traps form quasi-static charge distributions, most notably on the wafer surface or in the buffer layers underlying the active channel, act to restrict the drain-current and voltage excursions.

c. Interface defects: Heterojunction quality including the effect of AlN interface layer

The barrier/buffer interface is critical for device reliability. Imperfections in as grown material and those created during high field/temperature stresses can in fact be the source of the increased channel resistance. The wavefunction overlap with the barrier makes transport susceptible to the quality of the barrier and thus the defects. Hot carrier injection into the barrier will result in damage and will reduce the available channel conductance locally, leading to local heating and when combined with high fields to enhanced defect generation. To combat electron injection and the resulting anomalies, an AlN interfacial layer is introduced. Indeed the mobility measurements confirm the expected improvement. However, under RF stress nearly $\frac{3}{4}$ of devices having AlN interface layer as opposed nearly $\frac{1}{3}$ of those without it showed degradation [3,4]. *The bulk and interface defects that are generated due to the coupled forces of electric field, temperature and strain and which play a dominant role in device degradation have not been studied in detail and require further investigations.*

HOT PHONON EFFECTS

Existing defects and those generated by hot phonons and electrons, and high fields cause G-R noise which can be monitored with LF noise measurements [3,4]. This together with hot phonon effects (with temperature reaching 2000 K

at 50-60 kV/cm), [3,4] accessed by HF noise measurements and simulations, has been used to determine the nature of these defects as input for physics based modeling of failure. Strong electron-phonon coupling in GaN leads to hot phonon generation (some 30 X greater vs. GaAs) which is assisted by the inefficient LO phonon decay mechanism. The hot phonon/electron damage and phonon decay mechanisms which are also critically important for heat dissipation are not developed in GaN.

OHMIC AND SCHOTTKY CONTACTS AND THEIR IMPACT ON RELIABILITY

The best performance GaN HFETs is inconsistently obtained with significant dispersion from device-to-device, and from wafer-to-wafer. All high voltage GaN HFETs are affected and the problem is more severe as the device is scaled to reduced dimensions and the operating frequency is increased. The evolution of current and RF power reduction is generally a reversible process. However, the reliability is a strong function of gate leakage current, and that a ‘sudden reliability’ problem [2] exists when the field reaches a critical value, leading to permanent catastrophic damage. This has been attributed electron tunneling from the gate (drain side) to the surface, particularly when subjected to high terminal voltages [5,6]. It is shown that the reliability problem is due to electrons leaking from the gate electrode to the surface of the semiconductor [7].

Ohmic and Schottky contacts

GaN devices push metallization stability to their limit resulting in metallization degradation. Both the gate and drain/source metallurgy change including metallurgical phase change which is progressive and irreversible. Therefore, any complete model must take phase transformations and metal degradation into account.

The Ti/Al contacts are initially stable against oxidation and cracking when sealed with Ni/Au but degrade after prolonged operation. This is a wearout mechanism which can be rapidly revealed by accelerated life tests. Ultimately, an n^+ top layer on AlGaN barrier and gate recessing would be required to reduce contact resistivity and ensure current uniformity. Selective dry etching for gate recessing have already been explored [3,4]. Interdiffusion at metallic interfaces and possible electromigration from contact regions also produce defect generation which degrades the device performance. These processes can be properly modeled and simulated to determine the critical bias and channel current conditions which crucially affect the rate of the device degradation.

Field-assisted metal diffusion

The extent of electromigration is dependent on factors such as conductor-line properties and any inhomogeneities as well as structural features of the conductor layout. Naturally, electromigration has been studied since the magnitude of

defect transfer depends directly on the current density and poses a formidable challenge for GaN FETs. High temperatures, particularly by the gate and drain metallization, will result in mass transport facilitated by the short diffusion distance associated with defects, such as dislocations, grain boundaries, or external surfaces. It is therefore imperative that industry completes the understanding of mechanisms for electromigration and interdiffusion and transfers this knowledge to appropriate reliability models.

SUMMARY

Our effort has culminated in the development of physics based failure models for GaAs and GaN based FETs. More important an integrated fundamental science approach has been developed encompassing degradation processes such as the material/heterostructures, bulk, surface and interface states, temperature, strain, and high field effects such as hot carriers and hot phonons generation. The effect of hot electron and hot phonon on phonon decay and power dissipation as well as the velocity limiting processes can now be determined accurately. The nature of gate leakage current and its effect on reliability, which is somewhat temporary with long recovery time, will have an impact.

The effort has led to a comprehensive reliability physics model (drift-diffusion, electro-thermal, hot-phonon, and Boltzmann transport and charge control). The effort has led to the effective parameterization of the degradation mechanisms. With appropriate probability density functions the model can predict statistically meaningful lifetimes.

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ACRONYMS

HFET: Heterojunction Field Effect Transistor
2DEG: Two Dimensional Electron Gas

