Formation of Slanted Gates for GaN-Based HEMTs by Combined Plasma and Wet Chemical Etching of Silicon Nitride

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KEYWORDS: Slanted gates, SiN_x etch, phosphoric acid, plasma etch, wet etching, submicron trench

Abstract

We propose a new method for the formation of slanted gates for GaN-based HEMTS that consists of the combination of an anisotropic plasma and an isotropic wet chemical etch step. By combining these two steps, a slanted trench is formed in silicon nitride, followed by the gate metallization sequence. During the plasma etch step, the silicon nitride is only partially etched; the slanted profile is created during the wet etch process step. The ratio of plasma etch to wet etch determines the angle of the slant. This process was successfully applied to a HEMT structure consisting of an epitaxial layer of a 17 nm thick $Al_{0.25}Ga_{0.75}N$ barrier and a 5 nm thick GaN cap on a 4 inch n-type SiC substrate. The process yielded 280 nm long slanted gates. Electrical tests showed that 2x50 µm devices reached a typical maximum output current of 0.75 A/mm with a high fabrication yield.

INTRODUCTION

A commonly used technology sequence in the fabrication of GaN-based HEMTs and MMICs is the so-called "embedded gate" process, in which the gate metal is deposited into a trench opening in a dielectric passivation layer usually consisting of silicon nitride (SiNx). Control of the trench etching is of great importance, as the later semiconductor-metal interface at its bottom contributes significantly to the electrical characteristics and the reliability of the device. Plasma etching of SiNx can be performed with high and low bias levels. High bias processes are more anisotropic, but the semiconductor surface is more prone to damage or ion contamination. Low bias etching creates less surface damage, but isotropic etching causes a widening of the trench. A trapezoidal profile of the trench is highly desirable because it supports a void free metal filling and reduces dc-RF dispersion in AlGaN/GaN HEMTs by formation of slant field plates that diminish the peak electrical field under the gate [1,2].

In this work we present a novel process for the formation of slanted gate trenches. The critical etching step is subdivided into 2 steps: (1) a high or low bias plasma etching process to partly form the trench, i.e., the SiN_x layer will not completely etched down to the semiconductor interface, and (2) a wet chemical etch step with phosphoric acid to remove the remaining SiN_x and to generate the desired trapezoidal trench profile. The process sequence is shown in Fig.1. After nitride deposition covering the full wafer and trench lithography, the nitride is etched partially with a SF_6 based plasma process to retain the desired residual SiN_x thickness (steps a – b). Then, the resist is stripped (step c) and an isotropic wet chemical etch is applied to thin the nitride layer (step d) thereby forming the slanted sidewall. The transistor gates will be finalized by a 2^{nd} lithography followed by metal deposition and metal lift-off (step e). The ratio of the etch depths in the nitride layer by plasma and by wet chemical etching will determine the exact geometry of the gate trench. This allows for control of the sidewall angle. Etching, e.g., half of the nitride layer by the plasma process and the remaining half by the isotropic wet process will result in a gate trench with a slanted sidewall of 45 degrees.

a) Nitride deposition and lithography

b) Anisotropic dry etch process

c) Resist strip

d) Isotropic wet etch of nitride

e) Metallization

Fig. 1. Process scheme for the fabrication of slanted gates

If already 9/10 of the nitride thickness is removed by plasma etching, almost no slant will be obtained after the wet etch. In either case, as the plasma process does not touch the surface, plasma bias induced damage of the AlGaN (or GaN cap) layer will not occur. However, as the nitride is also etched away uniformly on the wafer, this loss has to be considered carefully when choosing the initial nitride thickness.

Nevertheless, this process scheme has some limitations. First, the resulting trench opening is always larger than the lithographical CD due to the widening by the isotropic chemical etch process; the CD of the lithography process is not preserved. Unless the required gate length is not too small this feature can be taken into account as the CD widening happens to be quite reproducible. Second, the selectivity of the etch with phosphoric acid with respect to the topmost epitaxial layer must be evaluated carefully. Changes in the composition of the AlGaN and the silicon nitride layer can lead to different etch rates; so the etch time and rates for the nitride layer need to be controlled carefully. Third, the selective measurement of silicon nitride on top of an AlGaN or GaN layer is not easily accomplished.

EXPERIMENTAL

All experiments were performed on 4 inch Si, GaAs and n-type SiC wafers with SiNx films deposited at 345 °C using a Sentech SI500D PECVD tool. The gates were processed in two lithography steps. For the trench layer, ARP 639.10 (PMMA 50k, layer thickness 600 nm) was used as resist. For the (lift-off) patterning of the metallization layer, a combination of ARP 639.10 (PMMA 50k, 500 nm) and ARP 679.04 (PMMA 950k, 300 nm) was used to generate the desired undercut. Exposure was done on a Vistec SB251 electron beam lithography tool with an acceleration voltage of 50 kV and a dose of 300 µC/cm². A Sentech SI500 ICP tool was used for dry etching of the SiNx layer by SF6/He. The wet chemical SiNx etching was performed with phosphoric acid (85%) at 140 °C. The nitride thickness after the etch steps was determined on non-structured silicon wafers with interference reflectometry in the range from 400 nm to 900 nm using an index of refraction of 1.98. The etch rate was calculated to be 9 nm/min (see results section). Size and profile of trench openings in SiNx were analyzed using scanning electron microscopy (SEM); a cross section of a slanted transistor gate was prepared by FIB. Electrical analysis of the transistors was performed on a Karl Süss prober with a Keithley 2420 source meter.

RESULTS AND DISCUSSION

Process development results

Wet chemical etch of silicon nitride films is a standard method in the silicon industry. Hydrofluoric acid, buffered hydrofluoric acid and hot phosphoric acid are commonly used etching solvents. The etch rate of hydrofluoric acid based solution is rather high, i.e., even at room temperature several 100 nm/min. Aqueous phosphoric acid dissolves silicon nitride according to the chemical reaction (1).

$$3\ Si_3N_4 + 19\ H_2O + 4\ H_3PO_4 \rightarrow 4(NH_2)_3PO_2 + 9\ H_2SiO_3 + 4\ H_2 \qquad (1)$$

The reaction rate is temperature dependent with an activation energy of about 95 kJ/mol in the temperature range from 130 °C to 200 °C. At 130 °C, the wet etch rate for thermal nitride is about 0.1 nm/min [4]. The reaction is selective with respect to silicon and silicon dioxide, both rates being lower by 1-2 orders of magnitude. The etch rate is very sensitive to the preparation method and the composition of the nitride films [5]. This requires the rate to be determined carefully for the respective nitride film. Eq.(1) also shows that the chemical dissolution reaction requires water as reactant. Hence, the concentration of the phosphoric acid, i.e., its water content, needs to be controlled, as water boils off during the etch process.

After having removed the silicon nitride, the reaction reaches the GaN surface that is also prone to an attack by phosphoric acid. About the same activation energy (87 kJ/mol) and comparable etch rates are reported; the reaction being self-limiting for selective planes [6]. This requires a careful selection and control of the overetch time.

In the processes a fresh solution of phosphoric acid of electronic grade (Aldrich, 85 %) was used for every batch. The wet chemical etch rate of silicon nitride films deposited at 345 °C was determined to be 9 nm/min on unstructured silicon wafers as base material at a bath temperature of 140 °C. To check for reproducibility, 4 test wafers were subjected to the process sequence. After deposition of 100 nm of silicon nitride, the photo resist mask was processed, followed by a fixed time plasma etch of 18 s to form the first part of the trench. Then, the resist was stripped with NMP and the phosphoric acid etch was performed.

A top down SEM micrograph obtained after the combined plasma and wet chemical etching is shown in Fig. 2. The top width of the trench is 390 nm, the bottom width is 291 nm and a symmetrical slant of 48 nm at both sides of the trench is observed. A SEM inspection and evaluation of 5 spots (top, left, right, bottom and center) on 4 wafers demonstrated a reproducibility of better than 5 % wafer to wafer and wafer within wafer.

In our processing scheme transistors were insulated by nitrogen ion implantation through silicon nitride. We found that such an implantation process changes the wet chemical etch rate of the silicon nitride. Fig. 3 shows the transition region from implanted to non-implanted region. The upper part has experienced isolation implantation, the lower part was covered with photo resist (3 µm) as implantation mask and has not seen any dose.

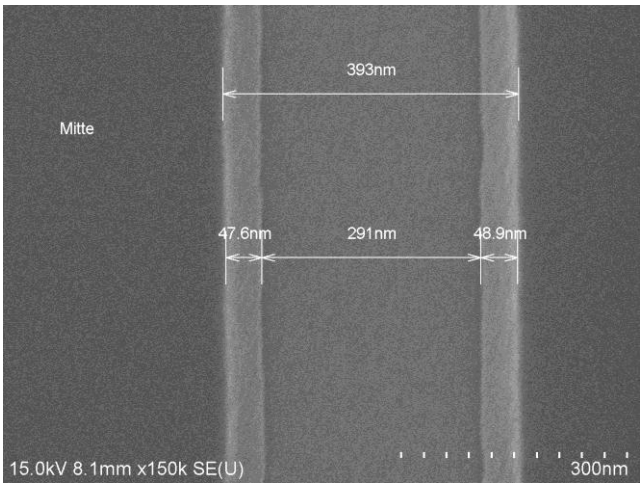

Fig. 2. Top–down SEM view of the slanted trench after combined dry and wet nitride etch

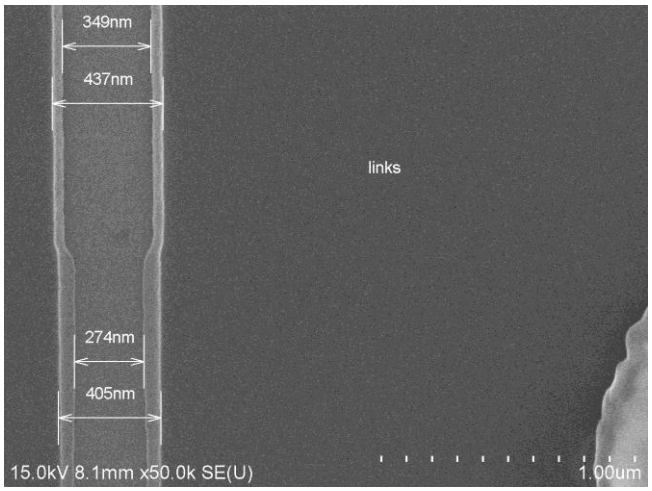

Fig. 3. Transition region implantation-no implantation after chemical etch. A widening in the implanted silicon nitride part of the trench is observed.

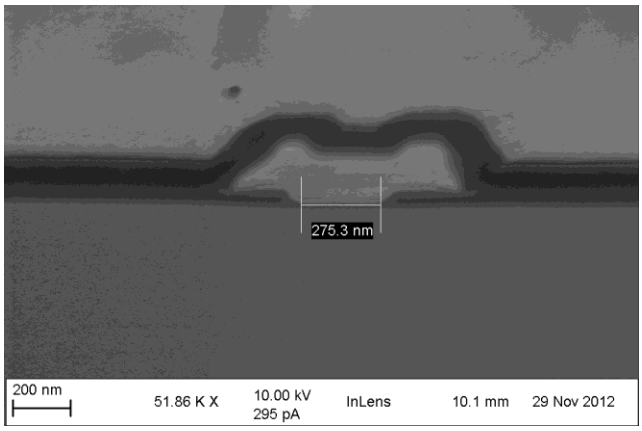

Fig. 4. FIB cross section of a metallized slanted gate on GaN wafer. The gate metal is covered by silicon nitride and a source connected field plate.

The top width changes from 405 nm in the not implanted region to 437 nm in the implanted region. We conclude that this implantation accelerates the wet etch process.

Results on process wafers with epitaxial layer

The slanted gate process module developed on test wafers was applied to wafers with a heterojunction epitaxial structure and the standard FBH process flow. This process consists of several modules. Only the gate module was changed. A wafer with an epitaxial layer consisting of a 5 nm GaN:Si cap and of a 17 nm $Al_{0.25}Ga0_{.75}N$ barrier grown on 4 inch n-type SiC was used as test candidate. Details of the epitaxial structure and processing are presented elsewhere [3]. Briefly, the gate is embedded in the first passivation silicon nitride layer of 150 nm thickness. During slanted gate processing this nitride was thinned to 100 nm. After gate metallization and deposition of another silicon nitride layer, a source connected field plate was formed. Fig. 4 shows a cross section of this gate stack prepared by FIB. The gate length (bottom opening) was measured to be 275 nm, the slant is roughly 55 degree. The smooth slant and the conformal metal fill is clearly visible.

Electrical testing revealed functionality of transistor devices. Fig. 5 and Fig. 6 show results of dc characterization of small two-finger transistors (2×50 µm). All but the center shot were functional; the latter was damaged during backside processing. The pinch-off voltage (V_{gs}) has a homogenous distribution with a mean value of -2.93 V and a standard deviation of 0.11 V (disregarding the two outliers in the upper left corner in Fig. 6). The measured output characteristics are typical for this epitaxial structure and a gate length of about 280 nm.

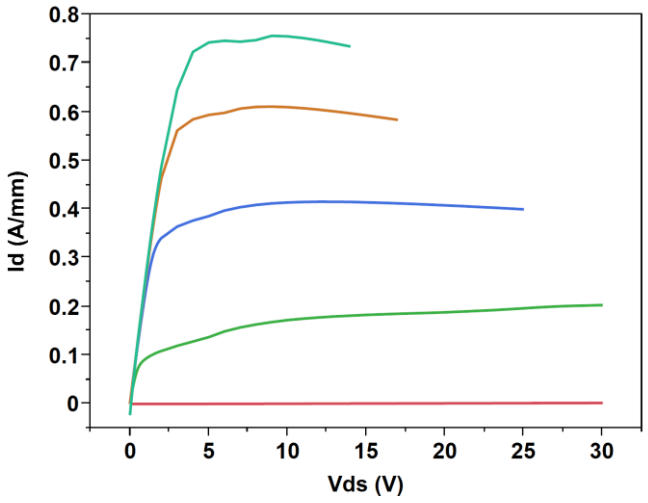

Fig. 5. Typical output characteristics of 2x50 µm devices on n-type SiC. V_G was increased in steps of 1 V from -3 V to +1V.

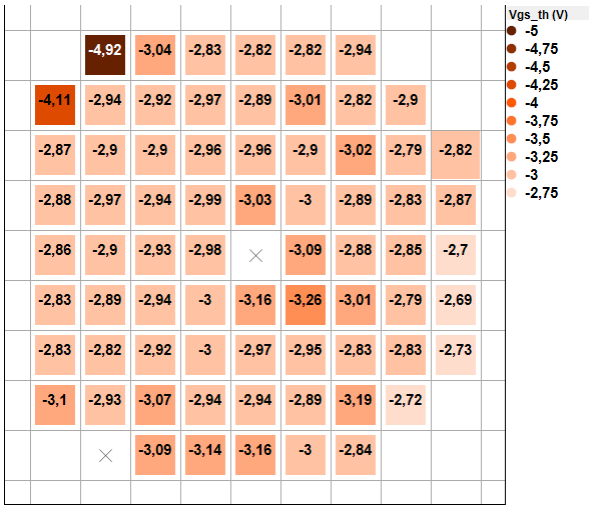

Fig. 6. Distribution of Pinch-off voltage (V_{gs} in V) across the 4" GaN HEMT test wafer

SUMMARY AND CONCLUSIONS

We have demonstrated a promising process for the formation of slanted gates. The process combines a partial anisotropic plasma dry etch with an isotropic wet etch of silicon nitride, avoids plasma damage of the semiconductor at the gate interface and generates the desired slant of the sidewalls.

ACKNOWLEDGEMENTS

The authors would like to thank the team of the process technology department for the constant support. We also thank Dr. U. Zeimer for the FIB preparation and S. Freyer for the electrical analysis of the test transistors.

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ACRONYMS

HEMT: High Electron Mobility Transistor
FIB: Focused Ion Beam
MMIC: Monolithic Microwave Integrated Circuit
SEM: Scanning Electron Microscope
CD: Critical Dimension