Heterogeneous Integration Schemes of Compound Semiconductors for Advanced CMOS and More-than-Moore applications

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Abstract

The continuation of Moore's law by conventional complementary metal oxide semiconductor (CMOS) scaling is becoming more and more challenging, requiring huge capital investments. On proposed scenario is the implementation of compound semiconductors as parts of advanced CMOS devices for More-than-Moore integration.

The continuation of improved performance characteristics in CMOS manufacturing is coming to a critical point, where electrical properties of silicon introducing a hard stop. One discussed route to increase performance is the heterogeneous integration of compound semiconductors into state of the art CMOS circuits. While growth of III-Vs on silicon shows limited success till now, as well as growing III-Vs in small trench structures shows to be challenging, direct wafer bonding overcomes these challenges.

Wafer bonding is the enabling process technology to make this happen. Two of the key wafer bonding techniques – low temperature fusion bonding as well as temporary bonding and de-bonding are the major subject of this contribution, introducing basic process flows and working principles for their CMOS integration.

HETEROGENEOUS INTEGRATION SCHEMES - INTRODUCTION

Most of today's applications rely on silicon. However, silicon has its limits. Especially when it comes to optoelectronics or high frequency applications, silicon has inherent material restrictions. Researchers came up with great new materials and device combinations. Major obstacles remain, though, how to facilitate this technology on low enough cost to everybody. Here, silicon technology, again, plays a major role, where yields are high and manufacturing is greatly optimized. One solution is to enable functions already at a substrate level by material engineering. These so-called engineered substrates enable new functionality and heterogeneous integration by novel materials or the combination of different materials for optimized device performance. Fusion of different functionalities on one chip is a central topic of engineered substrates.

As an example, nitride-based compound semiconductor devices show fast progress for light emitting diodes (LED), laser diodes, high-frequency transistors, power electronics and solar cells. The gain in efficiency and/or speed of these devices has mostly been enabled by recent advances in material design and growth technology. However, many applications are still suffering of reduced yield, a fact that is mostly stemming from reduced material quality and homogeneity. While high-quality substrates for homo-epitaxy are still expensive, alternative growth substrates show an offset in material properties such as lattice matching and coefficient of thermal expansion. As a result, the epitaxial film quality suffers a high dislocation density, resulting in reduced electrical and optical quality of the later-on devices.

Direct wafer bonding is a technology to join two substrate materials with different structural properties. Additionally, plasma activation of both wafer surfaces can be used to change the surface chemistry of both materials and therefore reducing the bonding temperature. In this way, materials supporting a high crystal quality of compound semiconductors can be joined with a carrier that accounts for differences in thermal expansion.

In this way, it is possible to have Si-based transistors side by side with high electron mobility transistors (HEMTs) made from GaN as an example. Similar process flows with different compound semiconductors are feasible as well.

While silicon is the most versatile material for producing highly dense, high-frequency logic circuits, GaN is attractive for high-frequency power handling in analog/mixed-signal circuits and for its green-to-ultraviolet optoelectronic properties.

Two bonding techniques offer essential benefits for the heterogeneous integration of compound semiconductors with silicon devices in a More-than-Moore approach, namely temporary bonding as well as direct wafer bonding. In the case of temporary bonding, thin layers can reliably be handled and transferred onto another substrate. On the other hand, direct wafer bonding allows a permanent layer transfer, for low defect compound semiconductor layer. Both these techniques are introduced in the following.

TEMPORARY BONDING

Generally speaking, temporary bonding and debonding is a process, enabling to attach a device wafer to a rigid carrier by adhesive bonding for processing. This processing can involve different back side processing, where the bonding layer protects the wafer front side. More common, temporary bonding is linked with thin wafer processing, where temporary bonding enables reliable thin wafer handling and processing without equipment modification. Figure 1 shows the general process flow for temporary bonding / debonding. Here, the product wafer which has gone through front end processing will be mounted onto a carrier wafer. The carrier wafer is coated with a temporary adhesive, which is usually deposited using spin coating processes. In figure 1, the materials involved in the temporary bond consisting of the temporary adhesive and any optional layers that will facilitate release of the carrier later on are summarized by the term *release layer*. For the bonding step, a key requirement is achieving accurate alignment of the product wafer on the carrier wafer to ensure that the product wafer will be supported properly during wafer thinning operations and backside processing. The temporary bonding step is succeeded by "back thinning and further processing" before debonding, cleaning and finally unloading.

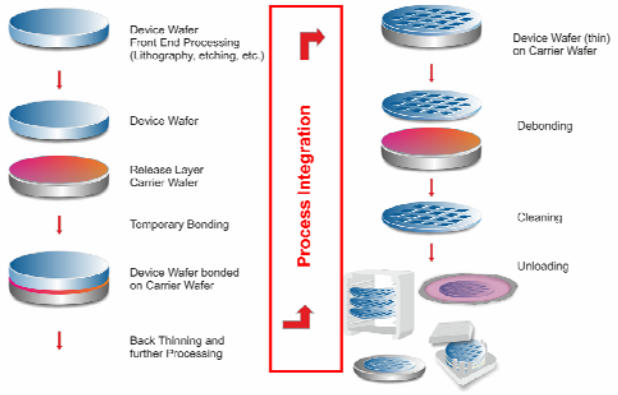

Figure 1. Generic Temporary Bonding / Debonding Process Flow

There are several ways to categorize the currently used temporary bonding technologies. Categorized from an adhesive perspective, there are two main options proposed in the market for temporary bonding and debonding. A first option relies on thermoplastic adhesives, while the other option relies on crosslinking adhesives. Thermoplastic adhesives offer the advantage of having the option to perform solvent cleaning after debonding to remove adhesive residues. Crosslinking adhesives do not offer such wet chemical cleaning capability and will have to be mechanically peeled either during the debonding operation or after debonding in order to remove the adhesive from the product wafer. Such peeling operation requires the adhesives to exhibit some degree of softness at room temperature in order to enable a reliable peeling process for removing the adhesive residue from product wafers that have topography such as solder bumps or copper studs. This softness is a major drawback, as it impacts wafer grinding and polishing operations adversely. This softness usually results in challenges in achieving uniform product wafer thickness in such thinning operations. For this reason, thermoplastic adhesives offer significant advantages in terms of cleanliness of the product wafer post debond and quality of wafer thinning due to the rigid support they can provide at room temperature. On the other hand side, thermoplastics will get soft when heated (as their viscosity drops along a given rheology curve), which may represent a limitation for certain applications. Nevertheless, this drop in viscosity is leveraged in the bonding operation to establish reliable bonding. The adverse effect of the drop in viscosity at elevated temperatures can be mitigated by using different adhesives for different applications. Today, there are thermoplastic adhesives available that offer by far the best thermal stability of any temporary bonding adhesive. A good example for that are the adhesives from Hitachi-Dupont Microsytems ("HD Microsystems") which exhibit thermal stability in the > 350°C temperature range. Most cross-linking adhesives are limited to < 300°C with most adhesives even being limited to about 250°C thermal stability when exposed to temperature for long time.

TABLE I
DEBONDING TECHNIQUES FOR THERMOPLASTIC ADHESIVES

Thermoplastic Adhesives – Debonding				
	Silicon	**Glass**	**Rigid**	**Room Temp.**
Solvent Release	**No**	**Yes**	**No**	**Yes**
Thermal Slide-Off	**Yes**	**Yes**	**Yes**	**No**
ZoneBOND® Debonding	**Yes**	**Yes**	**Yes**	**Yes**
Laser initiated Debonding	**No**	**Yes**	**Yes**	**Yes**

For thermoplastic adhesives, there are several debonding techniques available, ranging from solvent release debonding to thermal slide off debonding and most recently ZoneBond® debonding. Table 1 shows an overview of the various debonding techniques and some of their key requirements and properties as can be seen in table 1, solvent release debonding and laser assisted debonding require the use of glass carriers to enable debonding. On the other hand side, thermal slide off debonding requires elevated temperature to induce a drop in adhesive viscosity to enable sliding the carrier off the product wafer. The clear industry trend is to move to room temperature debonding methods. Another trend although not followed by the entire industry is the desire to use Si wafers as carrier materials as they integrate better into the entire fab environment [9]. For this

reason, ZoneBond® debonding is today the most favorable way of using thermoplastic adhesives in temporary bonding / debonding operations. EVG offers equipment solutions that support ZoneBond® debonding as part of EVGs LowTemp™ Debonding equipment and process portfolio within the EVG®850 equipment platforms (depicted in Fig. 2).

Another requirement for temporary bonding is the compatibility with topography. This essentially means that the adhesive must be able to embed topography as present on device wafers in the bonding interface. Temporary bonding techniques used today are compatible with those topographies and allow for creating adhesive layers of sufficient thickness so that the topography can be embedded. Both thermoplastic adhesives and cross linked adhesives are typically spin coated on either the device or the carrier wafer. Different spin coating recipes in conjunction with appropriate adhesive viscosities allow for adjusting the coating thickness to the required level. For cross-linked adhesives, usually a minimum thickness level needs to be maintained in order to enable peeling of the adhesive film as part of the debonding operation without the risk of tearing the adhesive film and leaving behind residue. This may be a disadvantage for applications with wafers without topography, as it prevents the user to take advantage of a thinner adhesive layer, which usually offers improved TTV of the adhesive. Thermoplastic adhesives, due to the different nature of adhesive removal post debonding by means of solvent cleaning usually do not have a minimum thickness requirement for the adhesive and therefore allow for optimized TTV values for wafers that have little or no topography. This lends itself towards wafers that are thinned to very low target thickness values. Thinning product wafers to target thickness values as low as 20 or 30µm has been routinely demonstrated using temporary bonding / debonding today.

Figure 2. This production platform for temporary bonding and debonding can accommodate up to 9 process modules.

DIRECT WAFER BONDING

As it has been already mentioned the introduction, direct wafer bonding has many advantages in comparison to direct growth of III-Vs on silicon. In many cases fusion wafer bonding uses Silicon dioxide (SiO_2) films on both wafers for the bonding process. The oxide films can be patterned or blanket. Fusion bonding requires flat wafers with a surface roughness of less than 1nm, which is well within the capabilities of today's CMP equipment. SiO_2 is a known CMOS-compatible material, and oxide deposition and CMP can be performed on practically all wafers. The resulting bond interface does not imply any limitations to further downstream processing, i.e., further processing steps can happen in a high vacuum or at temperatures higher than the bonding temperature itself.

Fusion bonding is actually a 2-step process consisting of pre-bonding and subsequent annealing. Pre-bonding is usually performed at atmospheric pressure. First the 2 wafers are brought in close proximity. Then a bond wave is initiated by a point contact usually in the center of the wafer. Pre-bonding gives sufficient bond strength for automatic handling and inspection of the bonded wafer stack. Annealing is usually performed as batch process.

The thermal annealing temperatures required are far too high for CMOS and III-V technology, in which the main temperature limitation is imposed by the metal temperature limits or interdiffusion (400°C or 450°C for very short time, in the range of minutes). The development of plasma activation of the wafer surfaces was the technical break-through which enabled the widespread use of fusion bonding for CMOS and III-V devices.

Low temperature plasma activated direct wafer bonding is a process that lowers the required annealing temperatures necessary for reaching high bond strength. One example for such an improvement is a pair of native oxide - thermal oxide wafers, where bulk strength can be achieved by plasma activation of wafers prior to bonding with subsequent annealing at 300°C for a short time (0.5 - 1 hour). Figure 3 shows the surface energy (bond strength) characteristics as a function of the annealing temperature for Si/SiO_2 wafer pairs with and without plasma activation prior to fusion bonding. The attempt to explain the newly obtained results using the known model for silicon hydrophilic bonding failed.

Comparison with the high temperature process shows that high bond strength values correspond to a state where all water is removed from the bonding interface. At this stage the bond strength is limited by the limited contact area due to the roughness of the surfaces. Starting from 200°C the nanogaps at the bonding interface are closed, so the surfaces are in full contact and bulk strength is reached [4].

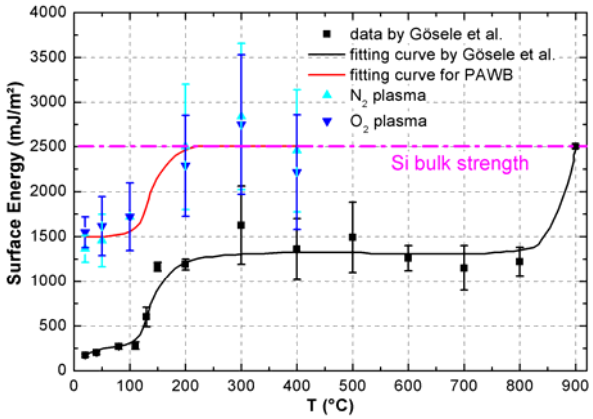

Figure 3. Surface energy of bonded Si/SiO_2 wafer pairs annealed at various temperatures for high temperature oxide bonding and plasma activated wafer bonding using N_2 respectively O_2 plasma. The maximum bond strength of 2.5J/m² is indicated by the dashed-dotted horizontal line. Data for high temperature process was taken from Ref. [3]

Fusion wafer bonding has several advantages compared to other bonding techniques. Pre-bonding happens at room temperature. As there is no thermal expansion of the wafers the achievable alignment accuracy is better compared to bond processes at elevated temperatures. Today alignment accuracies of better than 300nm (3σ) are achieved in high volume manufacturing. The pre-bonding process itself is very fast, which allows throughput of currently up to 15 wafers per hour per wafer bonding system. After pre-bonding the wafer stack can be inspected for bond defects and alignment accuracy. In case any parameter is outside of specification then the 2 wafers are just separated, cleaned and bonded again. There is no other wafer bonding technique that allows such an easy rework routine. Finally as annealing is performed as batch process the total cost-of-ownership (TCO) of fusion bonding is significantly better than other bonding methods.

CONCLUSION

Heterogeneous integration for advanced CMOS has caught a lot of attention recently. Despite the concentrated efforts to directly grow III-Vs onto silicon, dislocations are hard to control. Wafer bonding offers an ideal solution for this problem. Growing the compound semiconductor layer on another substrate and transferring this film marks the central process. This direct wafer bonding process enables high quality compound semiconductor films to be transferred on any substrate. In this way, different semiconductor layers can be stacked, enable to have different functionalities on one single wafer. On the other hand, temporary bonding facilitates the reliable transfer and processing of very thin compound semiconductor or silicon layer. In combination, temporary bonding and direct wafer bonding enable even flipping of a heterostructure. For example, in compound semiconductor devices the last layers are the most important one, carrying the device function. Direct bonding will move this layer to the bottom of the later device. Doing a temporary bonding step first, followed by a direct bonding step conserves the orientation and furthermore enables to remove or functionalize the growth buffer layer.
Today, temporary and fusion wafer bonding are both established technologies. Combining both techniques for advanced CMOS and More-than-more offers big potential for novel devices and increased functionality.

ACKNOWLEDGEMENT

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