Improvements to a mm-Wave GaN MMIC Process with Comprehensive and Efficient Process Control Monitoring

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Industrial use of GaN-based MMICs has increased significantly in recent years due to the potential of delivering high RF power at high efficiency. GaN MMIC components can significantly reduce size, weight power and cost requirements by delivering several times more power than competing technologies [1]. Production-level quantities are already being offered for low frequency GaN MMICs of less than 20 GHz [2]. However, there is a growing need for higher frequency, mm-wave parts up to 100 GHz.

HRL offers commercial mm-wave GaN MMICs that can achieve high output power at frequencies as high as 96 GHz [3]. HRL has seen demand for these high-frequency, high-power MMICs double in two years, and expects demand to continue to grow at this rate for some time. Therefore, HRL has established practices that will improve traceability, monitor processes, and improve efficiency, all while being scalable to meet the increasing demand. One of these practices, which will be covered in this paper, is a tightly controlled in-process wafer test plan with key performance parameter (KPP) screening and centralized data storage for quick and easy access for analysis.

HRL GaN MMIC wafers are tested in-process and in a cleanroom environment on automated probe stations at two processing steps. Wafers are tested just after FET gate fabrication, which is the first opportunity to probe devices that do not require airbridges. Wafers are then tested again at the end of frontside processing when devices that require airbridges and passive elements can be tested. Six to 11 discrete devices and over 40 passive elements are tested per reticle, and all wafer reticles are included in the test plan. The measurement definitions and test plans are setup and scripted in software to achieve automated probe station testing.

The raw measurement data is then imported into a MS SQL database. A Matlab script is used to process the raw measurement data and extract parameters. 20 key performance parameters and 148 total parameters are extracted from the raw data, which are also stored in the database. Parameters include standards such as Idss, peak transconductance and threshold voltage, but also process-sensitive parameters like leakage currents, trap data like current collapse, and performance properties like actual sacrificial breakdown voltage. Key performance parameters are automatically evaluated against pre-defined lower and upper specification screening limits to determine part failure and wafer yield. Overall process capability metrics (Cp, Cpk) are also evaluated based on the KPP specification limits.

The raw or extracted parameter data can then be viewed on-demand by all process engineers and staff through a web-browser-based user interface built using Visual Studio/C#. Data can be filtered and displayed in any of these formats:

- Lot summary table: Shows statistical data of extracted parameters of each wafer in a lot, including average, standard deviation, min/max, median, 25%/75% quartiles, individual parameter yield and overall wafer yield.
- Wafer maps: Shows a color-coded wafer map of a particular extracted parameter for an individual wafer (see example in inset of Figure 1).
- Trend chart: Shows a statistical box-plot of a particular extracted parameter across several lots and/or wafers, and data can be color grouped by lot, technology, etc. (see example in Figure 1).
- IV curves: Plots raw IV data from measurements, which can be color grouped by lot, wafer, etc.

- Yield analysis: Shows yield across several lots and/or wafers based on KPP screening criteria, along with failure mode analysis in the form of a Pareto chart.
- Pick list table: Shows a table of all parameter values of parts on a wafer for pick list generation.
- Correlation analysis: Allows correlation study of two extracted parameters from a selected data set.

This large amount of data has been useful for improvements through design feedback, process control verification, process technology comparison and problem troubleshooting. The statistical characteristic data is fed back into MMIC design for refinement and iterative improvement. Figure 1 shows an example of process control verification from a trend chart of Ft for recent wafers. The wafers are color-grouped by different epitaxial material sources, showing the stability of the process independent of source material. The average Ft was 90 GHz, and the average wafer standard deviation was 1 GHz. Figure 1 also shows an inset wafer map of Ft of one of the wafers included in the trend chart, showing an example of excellent wafer uniformity.

Figure 2 shows an example of how the database was used to compare process technology changes and improve device characteristics. A new gate process was used on a subset of wafers. Using the database of test data, over 1000 data points from the new gate process (Process B in Figure 2) were compared to thousands of data points from the original gate process (Process A in Figure 2). Percentage change in key performance parameters was analyzed to evaluate the new gate process. As shown in Figure 2, the only parameters that were significantly affected by the new gate process were gate leakage, drain leakage and DC-RF dispersion, or current-collapse. Furthermore, all of these significant changes were improvements: lower leakage and lower DC-RF dispersion. Therefore, by using the test database, the new gate process was statistically determined to be superior to the original gate process.

Finally, the database has been used to troubleshoot problems and diagnose issues. For example, at one time, device drain leakage current was increasing to undesirable levels. However, the leakage change was not consistent from wafer-to-wafer, which made the issue difficult to diagnose. The database was used to quickly find a strong correlation between device drain leakage current and epitaxial buffer leakage current. Furthermore, because X-ray diffraction data is gathered for all wafers, the database was then used to find a correlation between epitaxial buffer leakage current and epitaxial layer composition. Figure 3 shows how buffer leakage current changed with deviation of epitaxial material composition from the target value. Using this data, the epitaxial material screening criteria was tightened to minimize variation from the target epitaxial material composition.

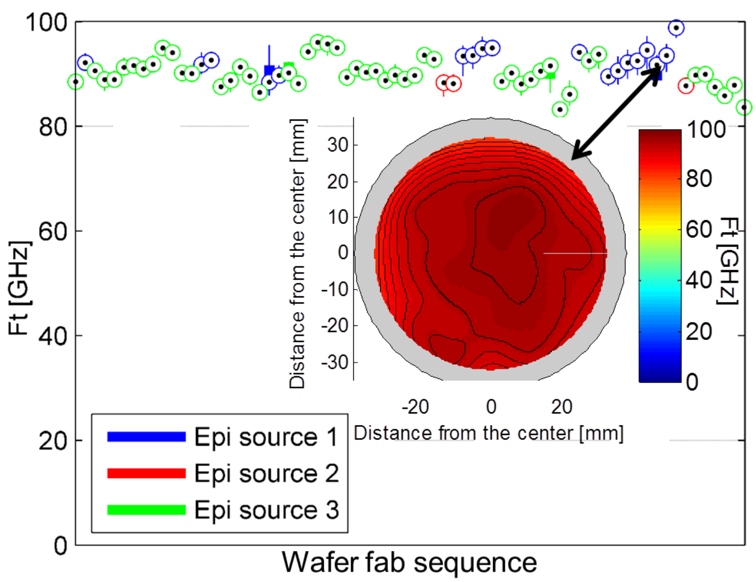

Figure 1: A trend chart box plot of Ft showing statistical box plots. Each column represents a wafer's statistical distribution. Solid boxes cover 25% to 75% of the distribution, and black dots indicate the median. The thin lines cover approximately 99.3% of the data distribution. Most

solid boxes and thin lines are not visible in this plot due to the tight parameter distribution. A wafer map is also shown in the inset showing an example of the excellent uniformity.

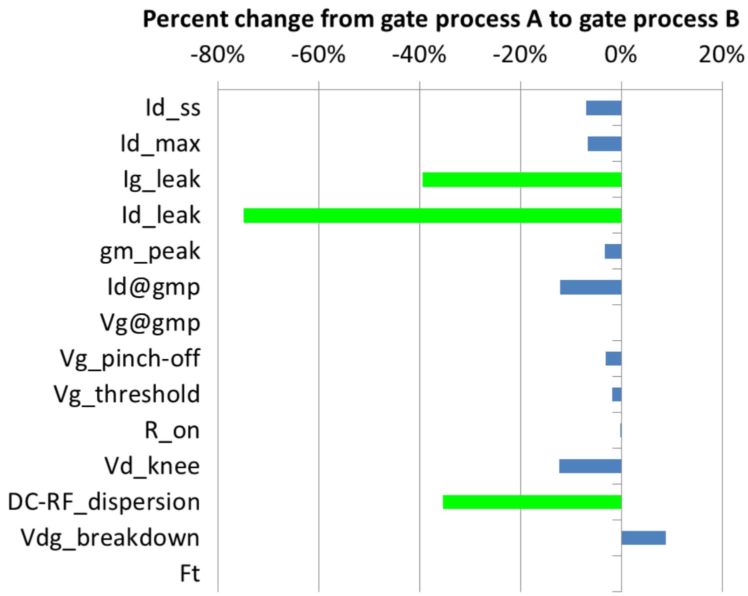

Figure 2: A bar chart comparing the percentage change of key performance parameters from the original gate process (A) to the new gate process (B). Green bars highlight significant changes. Only leakage currents and DC-RF dispersion were significantly affected by the processing change, and they were all improved.

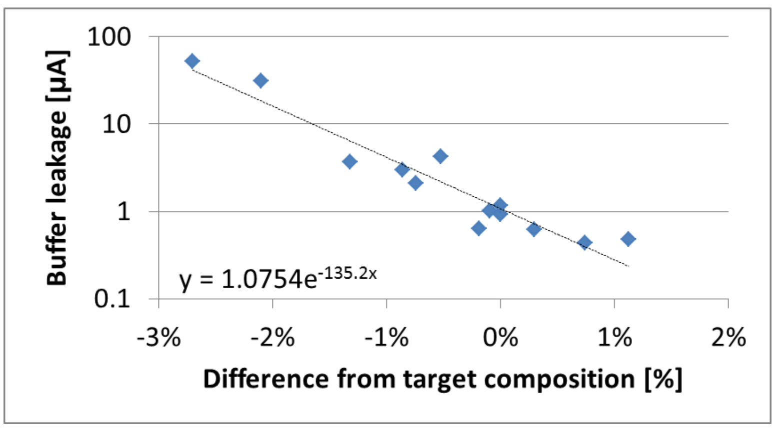

Figure 3: Correlation between wafer buffer leakage current and the difference from target epitaxial material composition, showing a strong relationship and fit with an exponential equation. This data was used to improve epitaxial material specification limits.

References:

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