# A new approach for GaN normally-off power transistors: Lateral recess for positive threshold voltage shift

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The power switching market for the automotive and transport industry, consumer and household electronics, manufacturing as well as energy generation, distribution and storage is rapidly increasing. Future systems will require transistors fabricated from nitride semiconductors in order to decrease volume, weight and cooling needs as well as to increase the overall efficiency. From a safety point of view it is highly desirable to use enhancement mode devices as these automatically turn-off in case of a failure in contrast to their depletion mode counterparts. GaN-based transistors are in general lateral devices that use the polarization-induced two-dimensional electron gas (2DEG) for electron transport which is modulated by a gate contact in between the source and drain contacts. The sheet carrier density increases with both the thickness and the Al-content in the AlGaN/GaN heterostructure that is grown on top of a buffer layer. Hence, transistors fabricated from this materials system are usually normally-on devices. In order to realize GaN-based normally-off transistors so far a gate recess as well as special plasma treatments or p-type layers underneath the gate contact have been pursued. These approaches have demonstrated normally-off devices but suffer from tight technological windows (epitaxy and processing) and complexities that complicate a reproducible fabrication of such normally-off devices.

Here, we propose a new approach for nitride normally-off transistors that is based on a recess etch in the source gate region in order to realize a positive threshold voltage with reduced technological complexity, see Figure 1. The process distinguished itself by a stable technological route for shifting the threshold voltage of a transistor. Starting point is a standard epitaxial and technological structure for normally-on devices having a continuous 2DEG between source and drain with an insulated gate using a dielectric between semiconductor and gate metal. The normally-off behavior is achieved using a recess etch of sufficient depth on the source-side of the gate, thus interrupting the 2DEG. Driving the gate contact into positive bias leads to carrier accumulation underneath the gate region and finally a current is flowing from source to drain once the gate voltage is large enough. Optional the recess is performed between two gate contacts (see Figure 1b) and carrier accumulation is performed utilizing the two gate contacts. In both cases a combination of a resist mask and the gate contacts as hard mask is employed for lateral definition of the recess.

We have realized such normally-off devices (see Figure 2) using standard epitaxial layers on 3-inch semi-insulating SiC substrates grown by metal-organic chemical vapor deposition having a 20 nm $Al_{0.20}Ga_{0.80}N$ barrier with a 3 nm GaN cap, a 40 nm $Al_2O_3$ gate dielectric deposited using atomic layer deposition, TiAlNiAu-based annealed ohmic contacts and a NiAu-based gate metal. Device isolation was done using Ar ion implantation. Single and double gates with lengths of 500 nm were defined using e-beam lithography whereas the resist mask was fabricated by optical stepper lithography. The gate-source and gate-drain spacings are 2 and 15 µm, respectively. The recess etch was carried out using a $Cl_2$-based dry etch for both the gate dielectric and the semiconductor layers.

The impact of different lateral recess dimensions for the technological options was examined using different layouts on the same wafer whereas different recess depths were realized using different wafers, see Figure 3. For the entire measurement region the gate current is below $10^{-9}$ A (50 µm gate width), evidencing that the gate dielectric is successfully working. We attribute the hysteresis of the drain current to surface traps generated by the dry etch for the recess as these samples were not passivated. The current ratio between on-state and off-state currents is around 7 orders of magnitude with on-state current densities of 250 mA/mm. With increasing recess depth the threshold voltage is shifting in the positive direction in agreement with our model as presented above. Furthermore with increasing lateral dimensions we do observe a drop in maximum current density which we attribute to high surface state density of the unpassivated recess area.

In order to investigate the high voltage robustness of our samples we have carried out breakdown measurements, see Figure 3c. For these measurements the gate bias was zero. Up to the breakdown voltage of around 700 V the leakage currents are below $10^{-8}$ A (50 µm gate width) demonstrating the high voltage stability of the structures. The breakdown voltage is in good agreement with normally-on devices with Schottky gates having the same gate-to-drain distance.

In summary we have presented and experimentally verified a new approach for normally-off transistors based on a recess leading to a laterally induced positive threshold voltage. Future work is directed towards passivation of the devices in order to reduce the impact of surface traps on device properties.

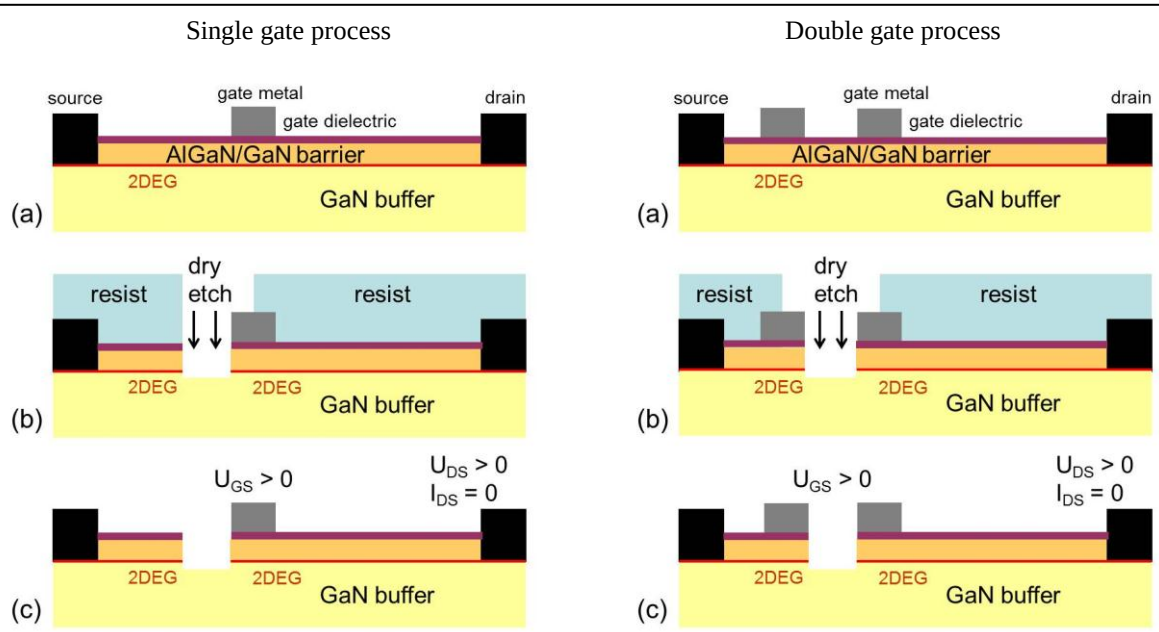


Figure 1: Schematic fabrication process and operation principle of the presented normally-off transistor using a single (images on the left) and double (images on the right) gate contact. The process starts with a planar semiconductor surface, source and drain ohmic contacts as well as an insulated gate contact as depicted in (a). A resist mask is used to define the area for the dry etch with the gates used as additional hard mask to define the dry etch into the semiconductor (removing the barrier partially or completely or even removing part of the GaN buffer), thus interrupting the 2DEG and leading to a blocking at zero gate bias as shown in (b). Once a positive bias is applied to the gate charge is accumulated near the gate contact (c) until the gate bias is large enough to allow a current from source to drain.

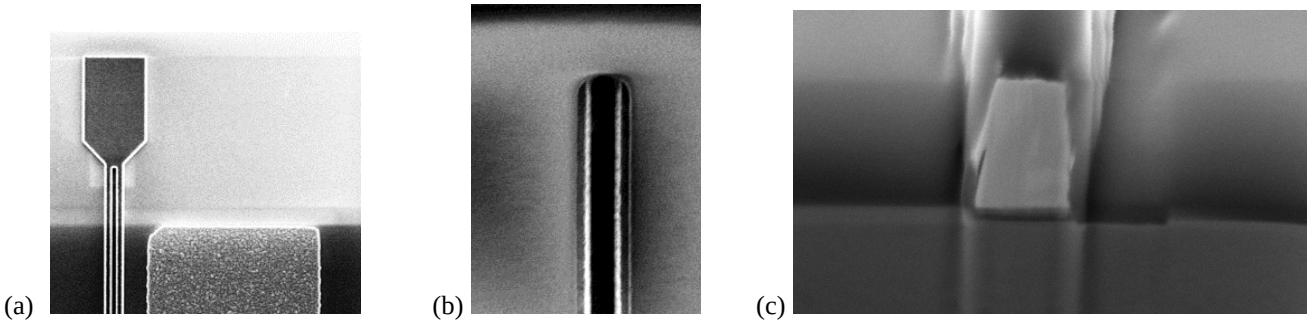


Figure 2: Fabrication process steps of a normally-off transistor with nominal recess widths of 400 nm: Double gate after gate metal lift-off (a), photoresist mask opening with the two gate fingers (b) and cross-section showing the recess for a single gate (c).

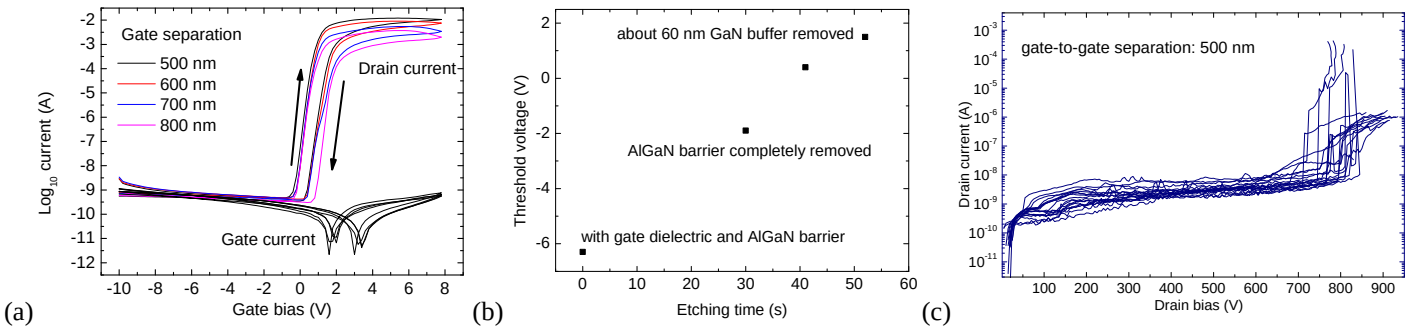


Figure 3: Electrical characterization of double gate test structures having a gate width of 50 µm: (a) transfer curves at 7 V drain bias for a recess etching time of 41 s, (b) threshold voltage vs etching time (gate dielectric and semiconductor) and (c) breakdown measurements at zero gate bias as mapping of a complete 3-inch wafer in FC-43 liquid to prevent breakdown through air.