Improved GaAs HBT Device Linearity with Flattened Cutoff Frequency Curve

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InGaP/GaAs heterojunction bipolar transistors (HBT) are widely used for wireless applications since they offer excellent features such as high power density and high efficiency. In addition, for many analog applications, the device linearity is paramount. This feature is best described by the intermodulation distortion, which is a key circuit parameter for these RF applications.

The intermodulation distortion (IM) and hence device linearity is well known to be caused by two major components from the HBT structure: (1) the transconductance (gm) and (2) the base-collector capacitance (Cbc).[1, 2] In this paper we will focus on a less investigated concept, that of the influence of the cutoff frequency (Ft) curve versus device current density flatness and its influence on device linearity.

Most of the device linearity studies have been focused on the variation of Cbc depending on the bias conditions,[3] the input signal, and the collector epitaxial structure.[4] The Cbc variation is less significant if both the doping and thickness of the collector are low so that the collector is fully depleted at low voltage. However, the resulting device breakdown voltage is low and not suited for current PA applications which require voltages up to 20V. As a consequence, alternate collector doping profiles were employed to maximize the breakdown voltage while maintaining the collector thickness and power capabilities of the device. Such profiles used either (1) doping spikes,[5] a thin higher doping layer placed somewhere within the uniformly doped collector, (2) step-graded collectors, and (3) collector doping ramps.[6,7] While the first method may generate more uniform Cbc profiles, all these methods enhance the device Ft at higher current densities, effectively delaying the onset of the Kirk effect. The delay of the Kirk effect has beneficial effects on the device linearity.

Fundamental device linearity studies have shown theoretically that the Ft curve vs. device collector current density (Jc) has an important role in minimizing the intermodulation distortion.[8, 9] The optimum distortion performance of the device is achieved when the Ft vs Jc curve is as flat as possible, i.e. the Ft vs Jc slope is as close to zero as possible. However, so far no experimental work has reported enhanced device linearity with a flat Ft vs. Jc curve through collector doping profile engineering.

In this work we employed all these collector doping profile engineering methods, i.e. doping spikes, step grading, and doping ramps to realize an Ft curve that is flat vs. device current density throughout the current density range of operation. Figure 1 and Figure 2 show a less abrupt Cbc device profile, especially at higher current density, close to the peak Ft. While these do not directly infer an improved intermodulation distortion, a look at the resulting Ft vs. Jc curve (Figure 3) shows a very flat Ft profile above a current density of about 0.1 mA/um^2. Figure 4 also shows less Ft peaking at low Vce and high current density. The resulting intermodulation distortion (Figure 5) is significantly less than with an epitaxial structure that has peaking Ft (non-flat). The onset of the lower intermodulation distortion corresponds to the same device collector current density where the Ft curve becomes flat.

In conclusion, with this work we report on a novel engineered Ft curve, a more flat Ft with current density, which results in improved device linearity. The new epitaxial structure is very well suited for applications where high device linearity is required.
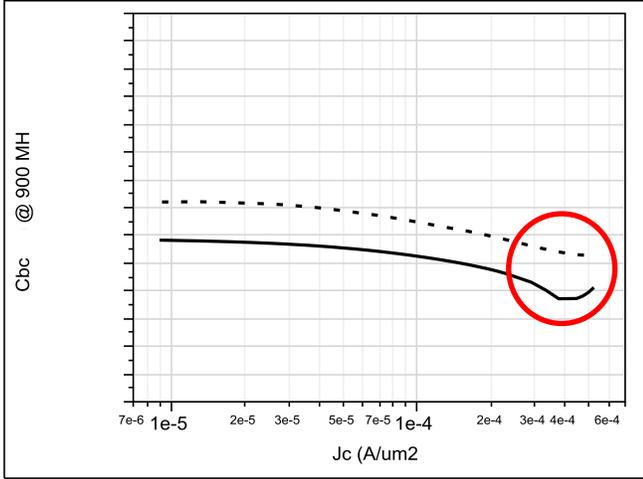
Figure 1. Extracted C_{bc} curve (arbitrary units, linear scale) versus device current density at Vce=1.5V, 900 MHz (dashed line is the improved structure).
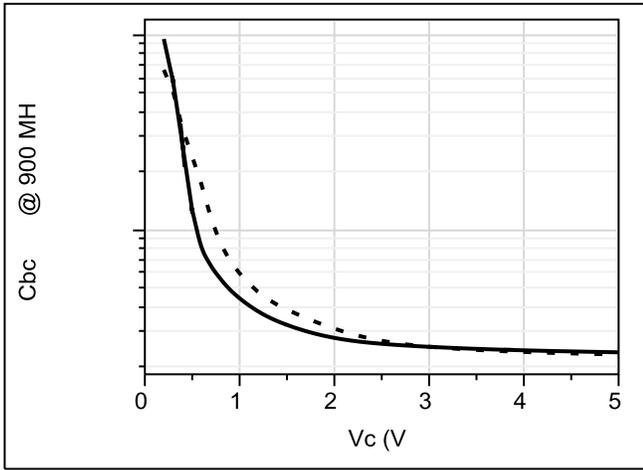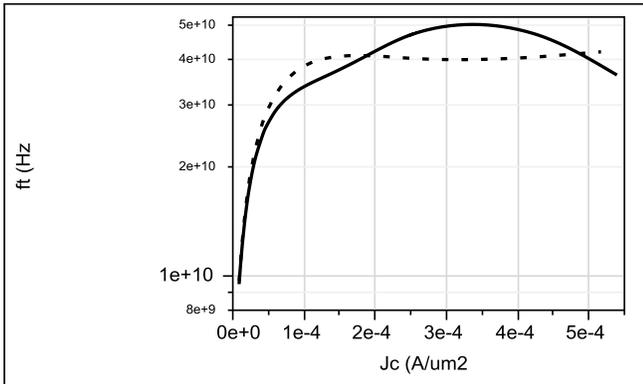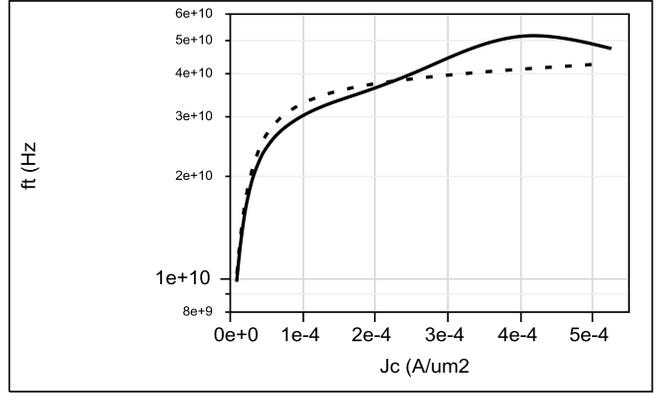

Figure 2. Extracted C_{bc} curve (arbitrary units, logarithmic scale) versus Vce at Jc=0.25 mA/um², 900 MHz (dashed line is the improved structure).

(a)

(b)

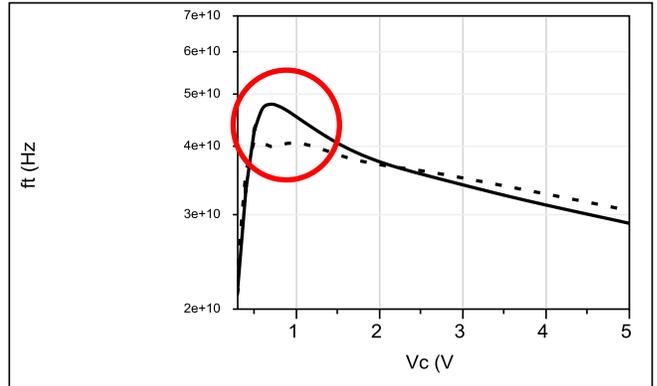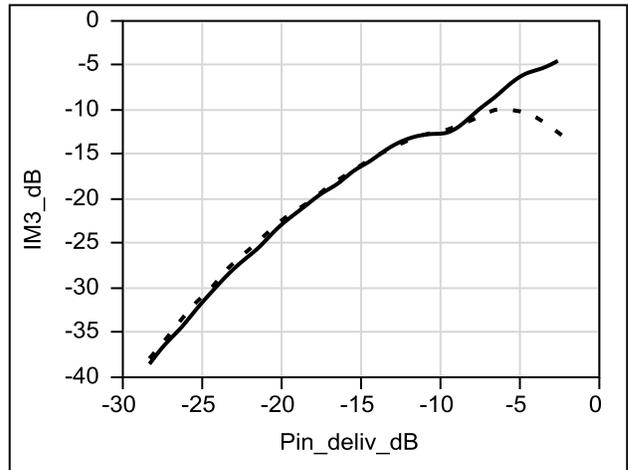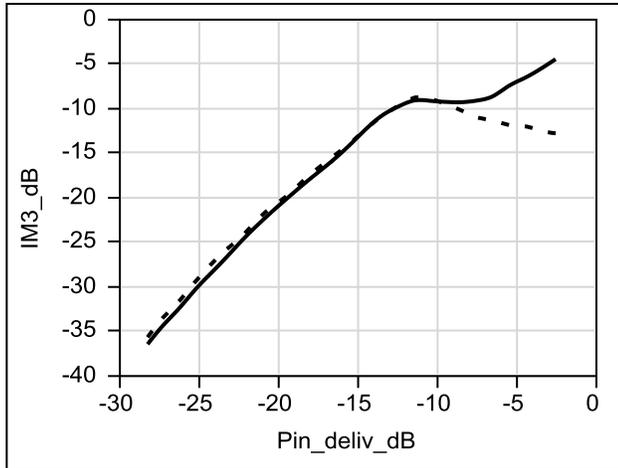**Figure 3. Ft vs Jc curve at (a) Vce=0.8V and (b) Vce=1.5V (dashed line is the improved structure).**

Figure 4. Ft vs. Vce curve at Jc=0.25 mA/um² (dashed line is the improved structure).

(a)

(b)

Figure 5. Intermodulation distortion IM3 vs device delivered input power for (a) maximum PAE tuning and (b) maximum Pout tuning.

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