An abstract submitted to CSMANTECH 2014, May 2014, Denver, USA: Homojunction GaN *p-i-n* Rectifiers with Ultra-low On-state Resistance

Homojunction GaN *p-i-n* Rectifiers with Ultra-low On-state Resistance

T.-T. Kao*, J. Kim, Y.-C. Lee, M.-H. Ji, T. Detchprohm, R. D. Dupuis, and S.-C. Shen

Center for Compound Semiconductors, School of Electrical and Computer Engineering
Georgia Institute of Technology, 777 Atlantic Drive NW, Atlanta, GA, 30332-0250
*POC: tkao6@gatech.edu

GaN *p-i-n (PIN)* rectifiers possesses several performance advantages over III-nitride heterojunction Schottky barrier diodes (SBDs) such as ultra-low leakage current and avalanche capabilities that are preferred for high-power switching applications. Using conducting free-standing (FS) GaN substrates, one may also enable a vertical power switch that allows for high-current-density handling capability with lowest possible conduction loss at a given blocking voltage rating. In this paper, we report GaN *PIN* rectifiers grown on a FS-GaN substrate that showed a breakdown voltage (V_B) of greater than 800 V and the off-state leakage current of fabricated devices remains below 1 pA (or $J < 1$ μA/cm^2) up to -200 V. The specific on-resistance ($R_{ON}A$) is 0.28 mΩ-cm^2 at the current density (J) of 2.5 kA/cm^2 And the corresponding Baliga's Switching Figure of Merit (FOM) is 2.5 GW/cm^2. The on-state resistance represents the lowest value a semiconductor power rectifier could achieve in the 800-V range.

The homojunction GaN *PIN* rectifiers were grown on a *c*-axis *n*-type FS-GaN substrate by a metal-organic chemical vapor deposition (MOCVD) system. The layer structure consists of a 1.1-μm n^+-GaN ($n = 1.5\times10^{18}$/cm^3), a 6-μm unintentionally-doped GaN drift layer, a 260-nm thick p-GaN ($p = 1\times10^{18}$/cm^3), and a 20-nm thick heavily doped p^+-GaN cap layer. The vertical GaN rectifier fabrication starts with a mesa etching, followed by a Ti/Al-based backside contact, a Ni-based *p*-type anode contact and the device passivation. Shown in Figure 1 (a) are the forward biased characteristics for a fabricated GaN *PIN* rectifier with an anode contact diameter of 30 microns. The turn-on voltage is ~ 3.3 V at $J = 10$ A/cm^2 and the ideality factor (n) is 2.0. The differential resistance (dV/dI) decreases with increasing J and is 39 Ω at $J =$ 2.5 kA/cm^2. The corresponding specific on-resistance ($R_{ON}\times A$) is 0.28 mΩ-cm^2. Shown in Figure 1 (b) is the reversed biased of the same device under the test. The leakage current is below 1 pA (or < 1 μA/cm^2) up to -200 V. The capacitance-voltage (C-V) measurement, shown in Figure 2, indicates that the net carrier concentration of the unintentionally doped GaN drift layer is 1.3×10^{16} cm^{-3}. Therefore, the reach-through voltage can be approximately estimated to be 480 V for a 6-μm-thick drift layer. The breakdown voltage (V_B) was also measured at the room temperature using a Tektronix 576 curve tracer. As shown in Figure 3, the device under test shows a leakage current of approximately 1μA at 800 V. The device breakdown is greater 800 V. Based on these measurement results, the Baliga's FOM ($V_B^2/ R_{ON}A$) is estimated > 2.5 GW/cm^2 . The FOM obtained in the homojunction GaN pin rectifiers shows clear performance advantages over vertical GaN SBDs (with an FOM of 1.7 GW/cm^2.) [1]

Figure 4 shows a competitive study of state-of-the-art GaN *PIN* rectifiers grown on different substrates[2-9], SBDs[1, 10-12] and normally-on AlGaN/GaN heterojunction field-effect transistors (HFETs).[13-19] The dotted lines on the plot represent the theoretical limits for Si, SiC, GaN switches. For a given breakdown voltage rating, vertical *PIN* rectifiers show at least a 10 times lower $R_{ON}\times A$ value when compared to III-nitride-based SBDs and AlGaN/GaN HFETs achieved so far. These *PIN* devices are consistently demonstrating the best Baliga's FOM for GaN-based switches and approaching to the theoretical limit for GaN. Our devices also demonstrated the same trend for GaN *PIN* rectifiers when it scales to the 800-V range and showed the lowest on-state resistance reported for 800-V devices to date. Further device fabrication processing and characterizations will be presented in the conference.

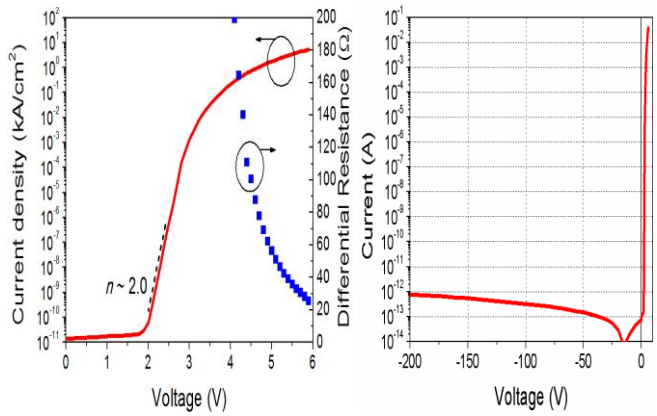

Figure 1 (a) The forward biased characteristics and (b) the reverse biased characteristics of a GaN pin rectifier with an anode contact diameter of 30 microns.

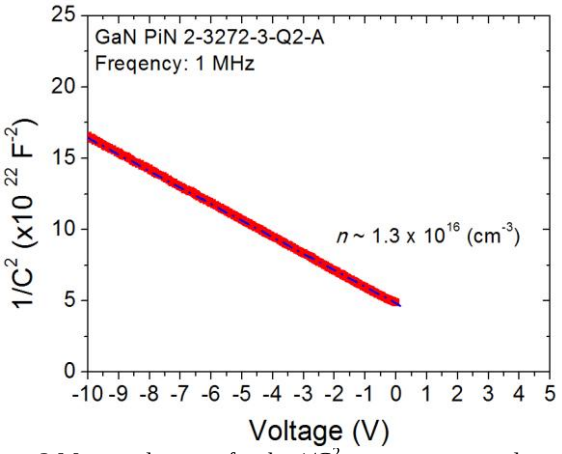

Figure 2 Measured curves for the $1/C^2$ versus reverse voltage of a vertical GaN p-i-n rectifier.

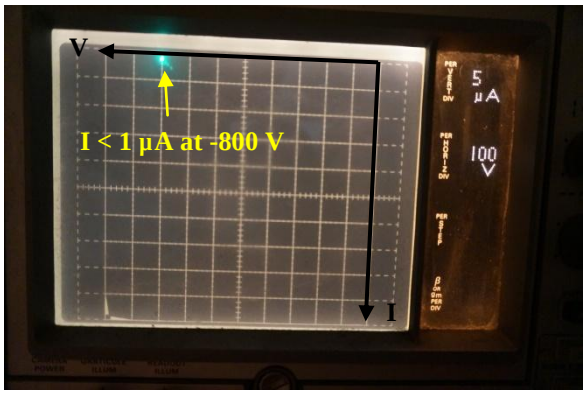

Figure 3 The off-state characteristics, as indicated by the bright dot, for a GaN p-i-n rectifier with an anode contact diameter of 30 microns.

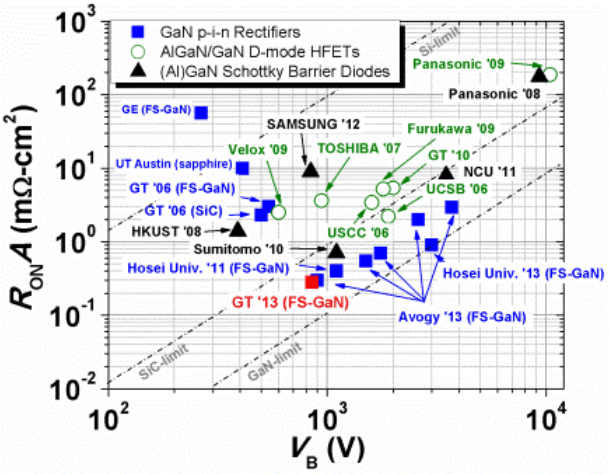

Figure 4 A comparison chart showing the breakdown voltage versus specific on-resistanc for GaN power rectifiers grown on sapphire, SiC and FS-GaN substrates, GaN or AlGaN/GaN SBDs and AlGaN/GaN HFETs.

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