Thermal Property of WNiSi Thin Film Resistor

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Abstract

Thin film resistor is a very important component in the integrated circuits for both Si and compound semiconductors. There are many different materials for different applications or processes. In this paper, the thermal property of a PVD deposited WNiSi is investigated. Correlations of as deposited film sheet resistance with annealing temperature and time are established. The activation energy is derived from the experiment data.

INTRODUCTION

Thin film resistor (TFR) is a component widely used in semiconductor integrated circuitry. There are many different types of thin film resistors, such as Cr [1], NiCr [2],[3], WSi [4]-[9], and TiN [10]. Their applications depend on their sheet resistance range and thermal properties. One of the most important parameters to describe the thermal property is the Temperature Coefficient of Resistivity (TCR). The TCR of each type of TFR has to be well understood before it is integrated into the wafer process and circuit design.

There is another interesting thermal property, which is the dependence of the as deposited film sheet resistance on the anneal temperature. For some of the TFRs, it is very important because improper thermal budget or large temperature variation during wafer process can cause large variation of the final sheet resistance. WNiSi is one of these TFRs and typically deposited in room temperature.

In this paper, we investigated the WNiSi thin film sheet resistance with different annealing temperature and time. A strong correlation between the sheet resistance and the heating temperature and time are established. The activation energy of WNiSi is determined. The mechanism of the sheet resistance changing with heating temperature and time is discussed.

EXPERIMENT

WNiSi thin film is deposited on a GaAs substrate which has a layer of SiO_2 for electrical isolation purpose. PVD system is used for WNiSi deposition at room temperature. The different thicknesses are used in the experiment. Then WNiSi deposited wafers were annealed in either an oven or a hot plate system. Figure 1 shows the simplified diagrams of these two heating systems. Figure 1(a) is a hot plate in a chamber with the pressure of 2.65τ. Figure 1(b) is an oven with N_2 flow. The thermal transfer in the hot plate system is dominated by thermal conduction, while the thermal radiation and convection are the dominated heat transfer mechanisms an oven. Therefore the heating is much faster in a hot plate system than that in an oven. Furthermore, the hot plate heating is more suitable for the study of WNiSi sheet resistance change with temperature range from room temperature up to 400°C. An oven is more suitable for the time dependence at a certain temperature.

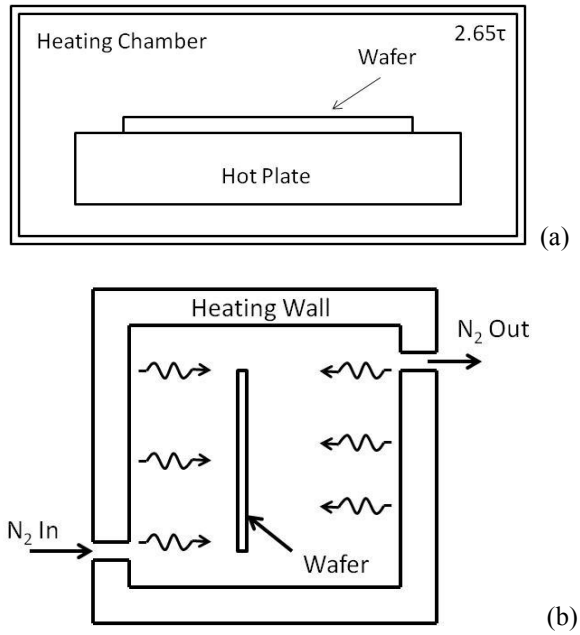


FIGURE 1 SIMPLIFIED DIAGRAMS OF TWO HEATING SYSTEMS: (A) A HOT PLATE IN A VACUUM CHAMBER WITH A PRESSURE OF 2.65τ; (B) AN OVEN WITH N_2 FLOW

RESULTS AND DISCUSSIONS

The sheet resistance was measured before and after the annealing process. For the convenience of the discussion of the sheet resistance at different temperature and time, the percentage change relative to the room temperature is used in the discussion below. WNiSi sheet resistance is a function of annealing temperature T and time t as $R\square(T, t)$. The percentage change of the annealed WNiSi sheet resistance change relative to the original value $R\square_0$ as the film deposition at room temperature is $\Delta R(T, t)/R\square_0$. Actually, $\Delta R(T, t)/R\square_0$ is $\Delta R[T(t), t]/R\square_0$ because the temperature can be also a function of time during the temperature ramping period.

Figure 2 shows WNiSi sheet resistance change as function of time as the annealing temperature of 250°C in an oven. X axis is the time in second and Y is in a scale of percentage. The normal annealing cycle is 30 minutes. For anneal time at 60 and 90 minutes, it will go through the annealing cycle two or three times accordingly. The TFR sheet resistance is measured prior to the first annealing cycle, between each annealing cycle and post final cycle. The correlation is shown as diamonds in the chart with a linear fitting. The interception gives the value of $\Delta R[T(t), t]/R\square_0$ at t=0 which is 17.4%. In reality, there is a ramping period for any annealing process. Therefore, the wafer temperature at T(0) is only about room temperature. In the case on oven annealing here at 250°C, the wafer temperature ramping is slow because of the dominated heat transfer mechanisms are radiation and convection and it will take about 7 minutes for the wafers to reach the set point of 250°C without over shoot. The square points are the data by removing the first 7 minutes from each annealing cycle. The linear fit also gives the same 17.4% interception. This means that the 17.4% change of the sheet resistance is coming from the impact of the temperature of 250°C, while the ~70 minutes at 250°C only gives another 2.4% change of the sheet resistance. In fact, the slope of the fit line, which is only 6ppm/s, describes the time dependence of the sheet resistance at 250°C.

The temperature ramping in an oven is slow and complicated, while it will be much faster with a hot plate heating. Figure 3(a) shows the $\Delta R[T(t), t]/R\square_0$ behavior with a hot plate anneal. The set temperature is 350°C. There are two regions in the chart. The zone I is a region of $\Delta R[T(t), t]/R\square_0$ fast growing, which is related to the temperature ramping. Since the time impact on the sheet resistance is only at ppm level, we can ignore the time contribution to $\Delta R[T(t), t]/R\square_0$ in this zone I. The zone II is a region of slow change. Therefore, $\Delta R[T(t), t]/R\square_0$ can be expressed as below:

$$\Delta R[T(t), t]/R\square_0 = \Delta R[T(t)]/R\square_0 + B*t \quad (1)$$

where B is the slope of the linear correlation in the zone II.

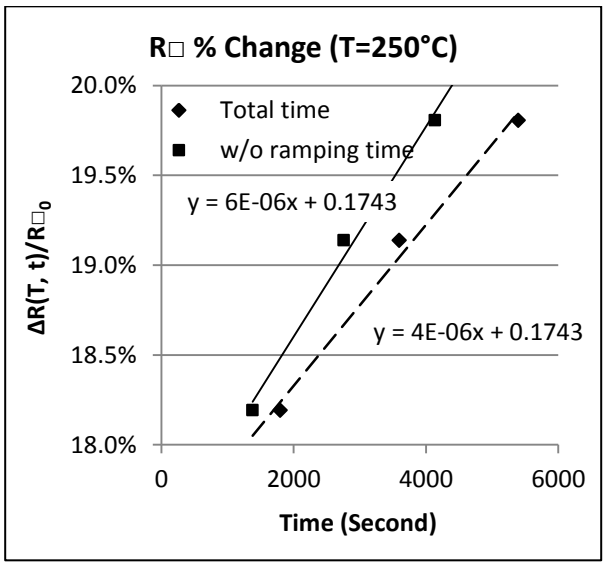


FIGURE 2 PERCENTAGE WNISI SHEET RESISTANCE CHANGE AT 250°C IN AN OVEN

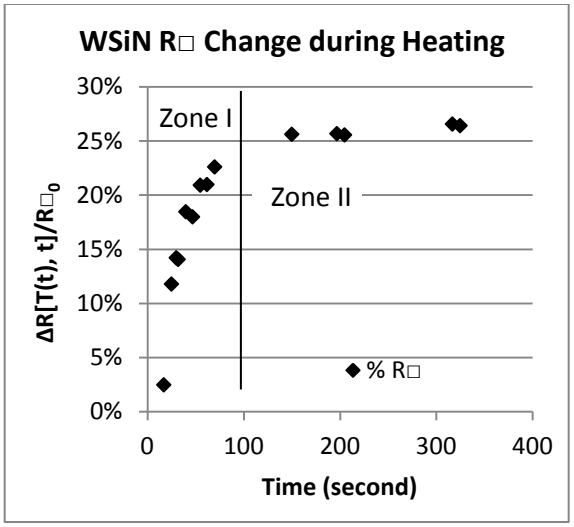
In a hot plate system, the heat transfer is dominated by thermal conductance. Because of the similarity of the thermal conductance equation and Maxwell's Equations, we can use a capacitor charging process to simulate the hot plate heating process. Then, the Eq. (1) can be written as

$$\Delta R[T(t), t]/R\square_0 = A*\{1-EXP[-(t-t_0)/RC]\}+B*t \quad (2)$$

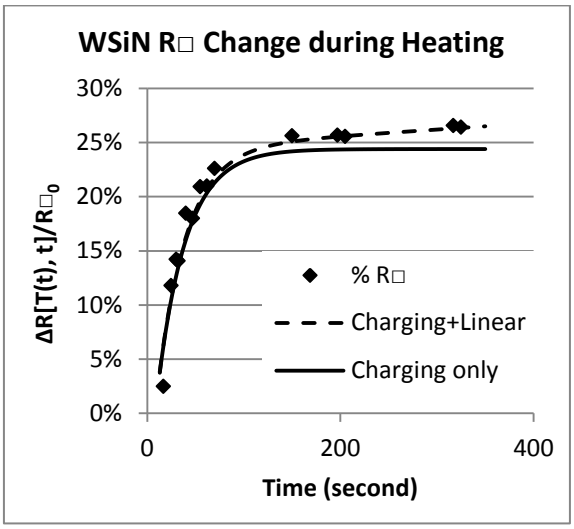
where A is the percentage sheet resistance change at the time the wafer reaches the hot plate temperature 350°C; t_0 is a time delay; R is the wafer thermal resistance and C is the thermal capacity.

The solid line in Figure 3(b) is a simulation with only the capacitor charging model, which will be saturated and will almost no change after the wafer reaches the set temperature. The dotted line in Figure 4(b) is the fit with the Eq. (2). The coefficient A in the Eq. (2) fitting is 24.4%, which is the impact of 350°C to the resistance change. The time constant RC is 30s, which is an indicator of how fast the wafer can be heated. WNiSi is deposited in a PVD with the room temperature on the chuck. However, the real film deposition temperature with the plasma strike is about 50°C. The delay time t_0 is the time for the sample heated up to the PVD deposition temperature of 50°C in order to have the sheet resistance change. In our case, t_0=8s. B=$4x10^{-5}$/s, which is the slope of the correlation to the time once the temperature is stable similar to the discussion for Figure 2. Although the slope here is almost one order higher than 250°C in the oven, it is still only 40ppm, which again proves that the time

impact to the annealing is a secondary factor comparing to the temperature.



(a)



(b)

FIGURE 3 WNISI SHEET RESISTANCE CHANGE DURING ANNEAL PROCESS. (A) RAW DATA AND (B) WITH A "CHARGING" MODEL FITTING

The temperature dependence of $\Delta R[T(t), t]/R\square_0$ is shown in Figure 4 with an activation energy Ea of 0.19eV. . The sample is annealed in the hot plate system with time of 300s and temperature from 300 to 400°C. A TEM cross section image of the sputter deposited WNiSi film is shown in Figure 5 as the dark area in the middle. Based on the target formation, it is a Si rich WSi_2 and $NiSi_2$ film and in amorphous form. This also can be seen from the XRD analysis shown in Figure 6. The sharp peak at about 16° on all three charts is from the substrate. The small wide peak at about 22° is from WNiSi film and indicates that there is only cluster of WSi_2 or $NiSi_2$ and there is no significant formation of hexagonal crystallization of WSi_2 as seen in CVD deposited WSi_2 film in Ref. [9]. The reasons of the difference are the lower anneal temperature range and the method of film deposition

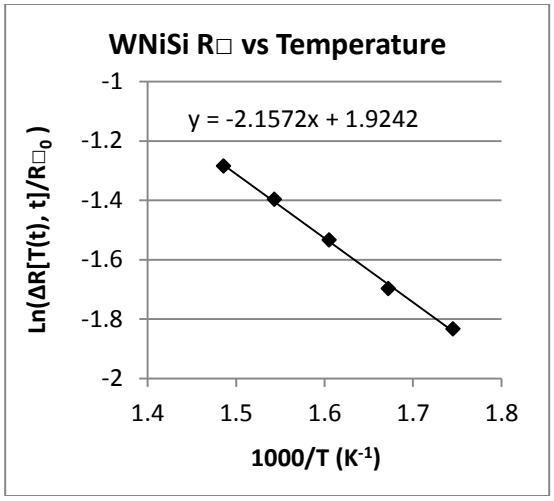


FIGURE 4 CORRELATION OF WNISI SHEET RESISTANCE AND TEMPERATURE

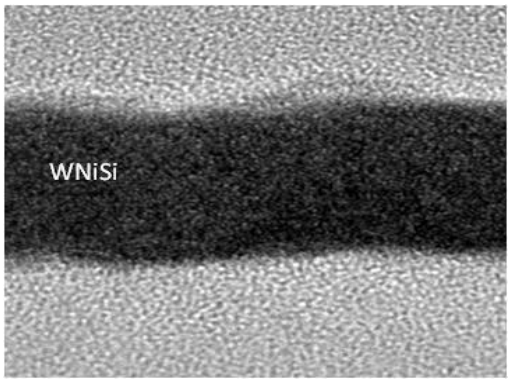


FIGURE 5 TEM IMAGE OF WNISI FILM

CONCLUSIONS

The thermal property of WNiSi is investigated. Its room temperature sheet resistance depends on the annealing condition. The annealing temperature dominates the sheet resistance change and the time is only with the impact of 6 to 40ppm/s in the temperature range of 250°C to 350°C. The activation energy of WNiSi TFR is 0.19eV. This property can be used for different applications, such as a thermal tunable resistor [11]. Fully understand of the sheet resistance change with temperature is still needed.

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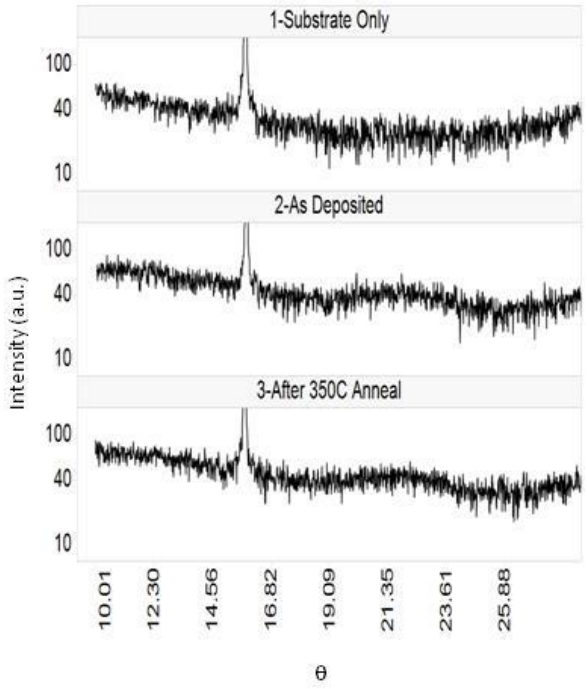

FIGURE 6. XRD ANALYSIS OF THE WNISI FILM DEPOSITED WITH A SPUTTER

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ACRONYMS

TFR: Thin Film Resistor
TCR: Temperature Coefficient of Resistivity
WNiSi: Tungsten-Nickel-Silicon
NiCr: Nickel-Chromium
WSi: Tungsten-Nickel-Silicon
TiN: Titanium Nitride
PVD: Physical Vapor Deposition
CVD: Chemical Vapor Deposition