Process Variations to Normally-off GaN HEMTs on Si with p-GaN Cap Layer

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Abstract

Effects of process flows and device structures on the electrical properties of enhancement mode high electron mobility transistors (HEMTs) are investigated in this work. Except the demonstration of high threshold voltage (V_{th}) of 4.3V, the process window of the p-GaN residual thickness to ensure a steady operation current was estimated to be 10±5nm in our case. However, to achieve a high breakdown voltage of 1630V, a precise control of 5nm residual is required to prevent the breakdown of p-GaN take place.

INTRODUCTION

GaN based high electron mobility transistors (HEMTs) on silicon substrates have received much attention in power electronics due to their low-channel resistance, high-breakdown voltage, and high switching frequency. However, the inherent normally-on behavior excludes GaN based HEMTs from most power electronic applications. Among the methods proposed to achieve enhancement mode (E-mode) operation, literatures on HEMTs using a p-type cap layer have reported the threshold voltage (V_{th}) ranging from 1V to 3V with the applied gate voltage larger than 5V [1-3]. Despite excellent performance reported, most works focused on demonstrating E-mode properties without comprehensive investigation on the correlation of the p-GaN layer structure with the electrical properties of an E-mode device, which is critical to ensure successful commercialization in the future.

In this work, the E-mode HEMT operation is demonstrated by growing a heavily-doped p-GaN cap layer on an AlGaN/GaN structure. The dependence of 2DEG carrier depletion and transport mechanism on the p-GaN layer thickness was studied by different process approaches. We conclude with an E-mode GaN HEMT with a large gate voltage of 10V and a high breakdown voltage of 1630V.

EXPERIMENT

The epi-structure was grown on a Si (111) substrate and is composed of a 2.4μm buffer, a 1.2μm GaN, a 10nm $Al_{0.25}Ga_{0.75}N$ barrier and a 60nm Mg-doped p-type GaN layer. Three process variations were employed. As Fig. 1 shows, Process A and B were designed for E-mode devices. For Process A, because the source and drain contact pads are positioned on AlGaN, the p-GaN cap layer on the source and drain was first removed by ICP-RIE before depositing the self-aligned Ti/Al/Ni/Au metal. After thermal alloy, Ni/Au metal stack was evaporated to form the schottky gate contact. Last, the p-GaN cap layer was etched to the desired thickness using the electrodes as the etching mask. For Process B, the p-GaN layer was first etched except the gate contact island. Then source and drain ohmic metal was evaporated and alloyed before schottky gate metal was deposited. To investigate the effect of p-GaN layer, Process C was performed with almost all the p-GaN cap layer etched. For all three types of processes, to prevent the etching damage to the AlGaN layer, we intentionally chose the etching depth to be either 45nm or 55nm. We design 5 devices with the nomenclature defined in Table 1. The gate–source offset length (L_{GS}), gate length (L_G), gate–drain offset length (L_{GD}), gate width is 2, 4, 6 and 50 μm, respectively.

DISCUSSION

The transfer characteristic of device A45L is shown in Fig. 2 and the V_{th} based on the linear extrapolation gives a value of 4.3V, which is the highest among the reports on AlGaN/GaN HEMTs using Ni/Au schottky metal semiconductor contact [1-3]. Alternatively, the V_{th} can be estimated by the gate bias at a drain current of 1mA/mm, rendering a V_{th} of 4.0 V. The origin of high V_{th} is mainly due to the thin AlGaN structure, which also lead to a low operating current of 32mA/mm at V_{GS}=10V. Since there typically exist 3~5nm residual p-GaN underneath the ohmic contact metal, device A45H, which adopted higher thermal alloy temperature can help to alloy through the p-GaN layer and achieve better contact resistance. The transfer characteristics show that the operation current of device A45H is 4.2 times higher than device A45L at V_{GS}=10V, and the V_{th} estimated from drain current of 1mA/mm will reduce from 4V to 1.5V. The detailed analysis shows that the alloy process will affect the barrier height between gate metal and p-GN/AlGaN/GaN structure.

For the devices using Process B, we further examine the dependence of electrical performance on the p-GaN residual layer with etching depths of 45 and 55nm. For comparison, Process C, which is similar to the conventional AlGaN/GaN HEMT structure, is fabricated with an etching depth of 55nm. The transfer characteristics of device C55H, B45H and B55H are shown in Fig. 3. The corresponding V_{th}, evaluated by the gate bias at a drain current of 1mA/mm, are -1.1, 1.6 and 1.7V, respectively. The 2.8V V_{th} difference between B55H and C55H indicates that the shift of V_{th} is related to the effect of p-GaN cap layer. Also, the transfer

characteristic of device B45H is very similar to B55H, showing that the additional 10nm etching has little effect on the carrier depletion in the channel and the process window of etching depth can be estimated as 50±5nm.

The breakdown measurement was carried out at the gate-source voltage of 0V due to the E-mode operation. The soft breakdown voltage at I_D = 1mA/mm of device A45L, B45H and B55H with L_{GD} = 6 μm are 257V, 448V and 566V, respectively. The gate island first (process B) process can achieve higher breakdown voltage and the 10nm additional p-GaN layer of device B45H leads to a lower breakdown voltage as compared to device B55H. To further investigate the effect of different etching depth and process conditions, Fig. 4 shows the device breakdown characteristics with respect to L_{GD}. For Process A or B, the breakdown voltages are almost independent of L_{GD} for the devices with the etching depth of 45nm, which means that within the L_{GD} range of discussion, the p-GaN layers dominate the breakdown behavior. As there are less residual p-GaN layers above the channel, device B55H have the largest breakdown voltage in Fig. 4, among which a breakdown voltage as high as 1630V can be achieved with L_{GD}=16μm.

CONCLUSIONS

E-mode GaN HEMTs were demonstrated with p-GaN cap layer and dependence of electrical properties on the process flow and device structure was investigated in this work. V_{th} can be adjusted by thermal alloy process and can extend to a value of 4.3V. The effects of p-GaN residual thickness were investigated and the process window to ensure a steady current is 10±5nm in our case. However, to achieve a high breakdown voltage of 1630V, a precise control of 5nm p-GaN residual thickness is required.

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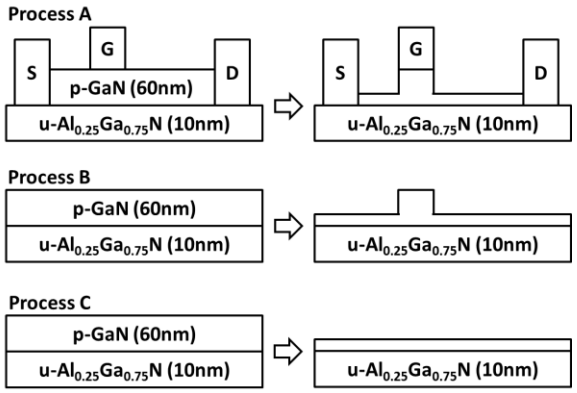

Fig. 1 Illustration of three types of fabrication procedures.

TABLE I
Process conditions of the devices using Process A, B and C

Device	Process	P-GaN etching depth	Alloy
A45L	A	45nm	850℃
A45H	A	45nm	900℃
B45H	B	45nm	900℃
B55H	B	55nm	900℃
C55H	C	55nm	900℃

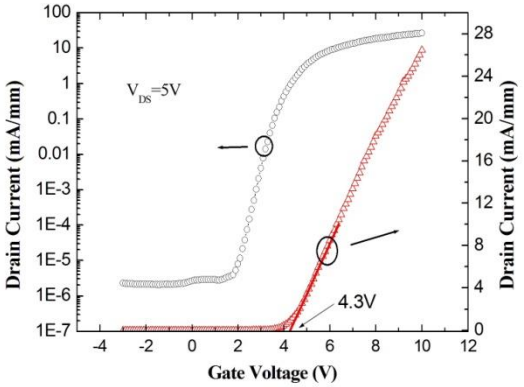

Fig. 2 Transfer characteristics of device A45L. The drain current is expressed in logarithmic (left) and linear (right) scale.

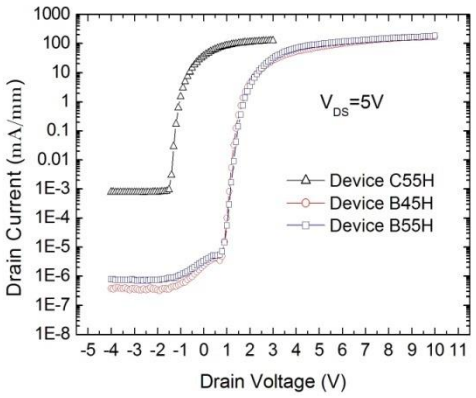

Fig. 3. Transfer characteristics of the device C55H, B45H and B55H

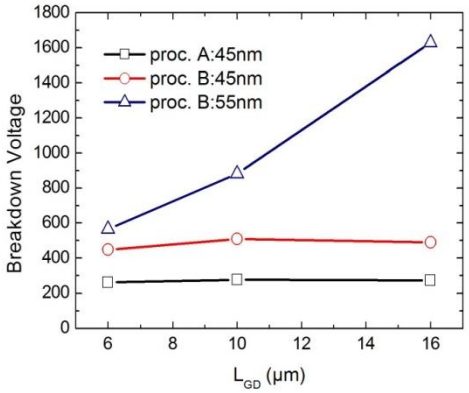

Fig. 4 Breakdown voltages of the devices with various L_{GD}. In this plot, devices fabricated using Process A and B are compared, along with 45 and 55nm etch depths for Process B.