A Mathematical Model to Determine the Impact of Through-Wafer-Vias on Backside Plating Thickness

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Abstract

While through-wafer-vias etched into the backside of semiconductor wafers appear to be very small, their combined surface area can have a significant impact on plated backside metal thickness. This paper reviews a model that predicts how the plating thickness changes based on via geometry and the total number of vias etched in a wafer. The model indicates what process changes are required to successfully match plating thickness across products with different mask designs.

INTRODUCTION

As part of a continuous process improvement effort, we wanted to tighten control of our backside plating thickness at our GaAs wafer manufacturing facilities in Newbury Park, California. This process plates several microns of copper on a thin gold and nickel-vanadium film that acts as a copper diffusion barrier. There is no mask pattern on the wafer during plating; the entire backside and etched through-wafer-vias are plated as a single sheet film.

One would expect that plating relatively flat surfaces would result in consistent plating thicknesses from one wafer to the next. Likewise, plating thicknesses should be very close across different products. Microscopic vias etched through the wafer were not thought to impact backside plating thickness control.

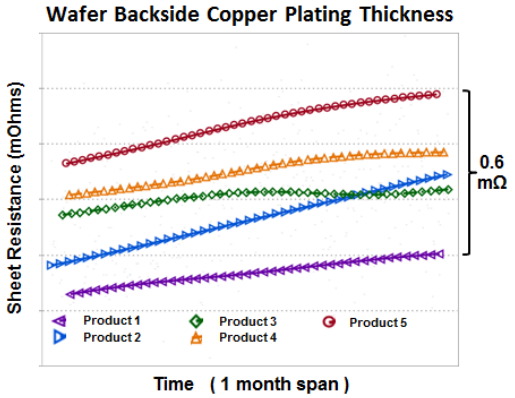

Figure 1: R_s of Backside Plated Copper vs. Time by Product

However, we noticed that plating thicknesses fell into distinct product groups as inferred by measuring the sheet resistance of the plated film. When the sheet resistance shifted, it generally shifted for all groups together, which indicated that the differences among products were independent of process variation attributed to plating bath and equipment parameter changes. The main difference among products was the number of vias on the wafer. Some had many tens of thousands of vias, and others had several hundreds of thousands. Surely this difference in the number of these tiny vias could not be the reason for these plating thickness differences, or could they?

A newly developed model revealed that not only the number of vias but also via dimensions, via surface roughness and wafer thickness all have a significant effect on backside plating thickness because of their impact on total wafer surface area. When these factors are incorporated into the model we can evaluate the impact of each factor and determine what adjustment to the plating time will compensate for the difference in plating thickness across different products.

DETERMINING THE MODEL INPUT VARIABLES

EXISTING VIA DIMENSIONS

A cross section profile of our vias shows a wineglass shape [Picture will be inserted in final paper]. This shape is defined by the photoresist pattern and via etch process steps. The photomask design starts with a rectangle opening on the mask. After exposure on a relatively low resolution contact aligner, the rectangle is printed with rounded corners. After patterning, a bake step heats the resist until it flows. This rounds out the edge of the via pattern to form a slope around the via opening. When vias are etched the photoresist around the via opening blocks the etch gases to transfer the initial patterned via dimension into the wafer substrate as a hole with near vertical walls. As the etch continues the resist is slowly eroded. The via opening increases in size allowing the etch gases to widen the etched hole dimension. Etching continues until the semi rectangular opening at the bottom of the via reaches the length and width of the designed dimensions. This gradual and continuing resist erosion and etched hole widening generates a slope at the top of the via sidewall profile.

To be able to estimate the surface area in a via this profile and the via dimensions must be incorporated into the model. Once one via has been modeled, the sum of surface area of all vias combined with the surface area on the back of the wafer defines the total surface area to be plated.

Starting at Square One With a Rectangle

The model starts with the assumption of a perfect rectangular via, using via dimensions from the mask design before the vias are patterned and etched. The model assumes the via wall profile is linear with the top opening larger than the bottom floor to form a trapezoidal prism (see Fig 1).

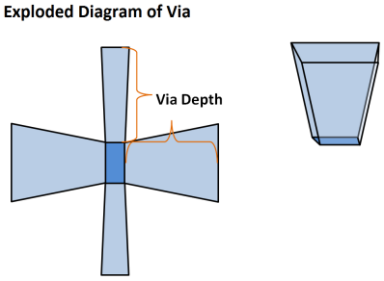

Figure 1: The Via Model Starts with A Trapezoidal Prism

The top and bottom via dimensions are determined from actual wafer measurements using a focused ion beam scanning electron microscope (FIB SEM), and the wafer thickness is the height of the prism. The area of the sidewalls and bottom of this prism are the first estimate of the surface area of one plated via.

The first correction to this estimate changes the shape from a rectangle to a standard ellipse. The ratio of the perimeter of the ellipse to the rectangle is used a correction factor to the surface area of the bottom of the via. Likewise the elliptical shape is propagated from the bottom to the top of the via, so this same ratio can be multiplied by the total surface area of the via walls to determine the surface area of a sloped elliptical via.

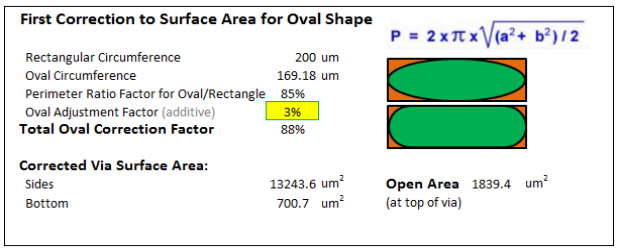

Figure 2: Elliptical and Oval Corrections to the Rectangular Via Model

A further correction changes the shape to more closely match the actual via horizontal profile to form an opening with rounded corners (see Figure 2). This adjustment is somewhat subjective based on examining vias on products that have been etched.

Because vias openings are very deep and the opening is narrow, plating tends to be thicker at the top of vias and thinner at the bottom. As metal ions in the plating bath first flow quickly and then diffuse slowly toward the bottom of the via they are more likely to plate the top of the via. This results in plating thicknesses at the bottom of the via that tend to be only a fraction of that on the back of the wafer.

The model adjusts for this difference by applying a second correction factor which estimates the sidewall plating thickness as an average linear change from the top to bottom sidewall of the via. The estimate is based on existing plating thickness measurements from FIB SEM cross sections.

The thickness estimate of the sidewall multiplied by the via surface area generates the volume of plating for the via sidewalls. The plating thickness at the via floor (also estimated by FIB SEM cross section measurements) is multiplied by the bottom rounded rectangular area to determine the plating volume at the base of the via. Combining both of these volumetric results establishes the first estimate of the plated metal volume inside one via.

Backside Plating Volume

The plating volume on the back of the wafer is determined by subtracting the surface area of the top of all via openings from the total area of the plated wafer diameter and then multiplying it by the targeted plating thickness (based on FIB measurements).

Combining the backside plating volume with the total plating volume of one via multiplied by the number of vias on the wafer results in a first order estimate of plating volume for the wafer.

The Full Paper Will Show

Using theoretical sheet resistance and the number of vias on each product, the model can predict the plating time change required to standardize thicknesses.

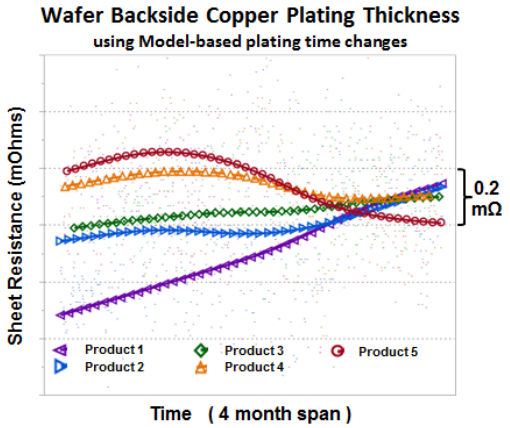

Figure 3: R_s of Plated Copper using Model-Based Plating Time Changes

Sheet resistance data collected from thousands of plated wafers with differing number of etched vias were used to fine tune original subjective correction factors, such as the oval adjustment factor and wafer roughness adjustment factor. Implementing model based plating time changes

resulted in a significant reduction in wafer to wafer backside copper thickness variation across all products (See Fig 3).