# Advanced bonding techniques for photonic integrated circuits

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## INTRODUCTION

Wafer scale or chip scale integration of compound semiconductors allows the implementation of high performance devices on a low cost silicon platform. This gained a lot of interest in versatile fields as electronics, optoelectronics, spintronics, biosensing, and photovoltaics.
Focusing on photonic integrated circuits (PICs), which are based on SOI fabrication infrastructure, heterogeneous integration of III-V materials, such as indium phosphide (InP), enables high performance devices at low cost and high volumes. The SOI platform is compatible with CMOS technology and hence is highly accurate and mature, leading to a robust, high-yield and reproducible technology and hence performance. Heterogeneous integration gives this platform access to high-speed and efficient III/V-based photonic components [1].
In this way the hybrid silicon platform heterogeneously integrates III/V functionality on the SOI platform by means of molecular wafer bonding. In particular fusion wafer bonding has been proven to enable sufficient bonding without degrading optical performance of the III-V materials and efficient optical coupling to the SOI waveguides.

## FUSION WAFER BONDING

Fusion wafer bonding is a two-step process consisting of a room temperature pre-bond and an annealing step. Traditional annealing processes developed for SOI wafer manufacturing required an annealing temperature of 1100°C. A new surface treatment with plasma activation allows reducing the temperature to 200-400°C. This makes fusion wafer bonding compatible with fully processed CMOS wafers. This fusion bonding process can be easily adopted for compound semiconductors with a pre deposited $SiO_2$ layer on top. Fusion wafer bonding has several advantages compared to other bonding techniques, which makes it particularly suitable for PICs. Pre-bonding happens at room temperature and therefore there is no thermal expansion of the wafers and the $SiO_2$ interface is compatible with the required optics. The pre-bonding process itself is very fast, which allows throughput of currently up to 15 wafers per hour per wafer bonding system. After pre-bonding the wafer stack can be inspected for bond defects and alignment accuracy. In case any parameter is outside of specification then the 2 wafers are just separated, cleaned and bonded again. There is no other wafer bonding technique that allows such an easy rework routine.

*Figure 1: Fusion wafer bonding process flow*

Finally as annealing is performed as batch process the total cost-of-ownership (TCO) of fusion bonding is significantly better than other bonding methods [2].

## PLASMA ACTIVATION

Figure 2 clearly shows that high surface energy and therefore good bond strength is achieved by oxygen plasma activation. The optimiziation of this process is investigated for differnet annealing temperatures. Further more it is demonstrated that lower annealing temperatures can be offset by extending annealing duration. Thus plasma activation is enabling heterogeneous integration of different materials with diverging thermal expansion coefficents, e.g., indium phospide (InP)-on-Si or gallium arsenide (GaAs)-on-Si by implementiation of a thin $SiO_2$ interlayer.

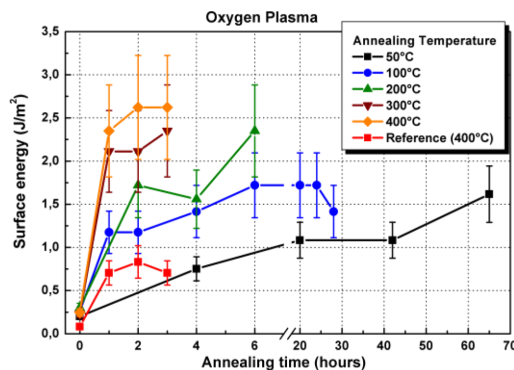


*Figure 2: LowTemp™ plasma activation with oxygen plasma enables high bond strength at moderate annealing temperatures.*

## ADVANCED CHIP TO WAFER BONDING

As in many designs of PICs only require heterogenous integration on a minor part of the SOI wafer costs can be significantly reduced by a chip to wafer approach. Costs can even be reduced further by applying advanced chip to wafer (AC2W) bonding techniques with a wafer level approach. This is especially the case as in contrast to wafer to wafer fusion bonding for chip to wafer heterogenous integration additionally to plasma activation still bond force and elevated temperatures are needed to gain sufficient bond strength and high yield.

The AC2W bonding process is a process flow for chip to wafer bonding especially designed for application of force while forming the bond at a throughput appropriate for volume production. The concept of separation of aligning substrates and then bonding the substrates to each other is well known and widely used for wafer to wafer bonding. At the AC2W bonding process the same concept is adapted to chip to wafer bonding. The AC2W process is a two step process as depicted in Figure 3. First all chips are aligned and tacked to the wafer, second all chips are bonded in parallel simultaneously permanently to the wafer [3].

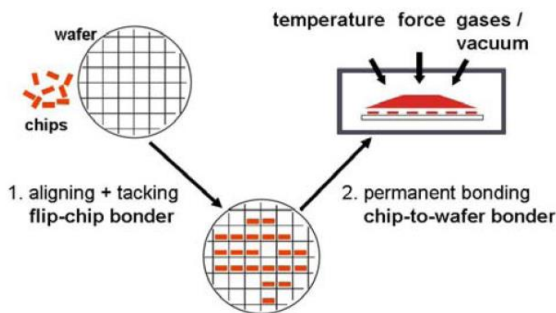


*Figure 3: The AC2W process flow*

For better understanding here an example will be given. It is assumed that 2641 chips with a size of 5 x 5 mm² are bonded to a 300 mm wafer. An interconnection time of 20s for bonding is assumed and additional alignment time on a flip chip is about 0.5s. It has to be mentioned that for heterogenous integration the bonding time can be significantly longer. This means that at the flip chip bonder only process each individual die needs (20s + 0.5s =) 20.5s to be bonded to the wafer which results in a throughput of about 175 dies per hour or 0.066 wafer per hour.

At the AC2W process the throughput of the two steps has to be evaluated separately. At the first AC2W step the throughput is determined by the flip chip bonder alignment time (0.5s) and therefore about 7200 dies per hour or 2.73 wafers per hour. Besides the throughput there are several variables that affect the cost of ownership of the AC2W process, as the die size, wafer size, bond process and alignment accuracy. For the given example the cost of ownership (CoO) was calculated and it shows a cost advantage of one order of magnitude as shown in Figure 4.

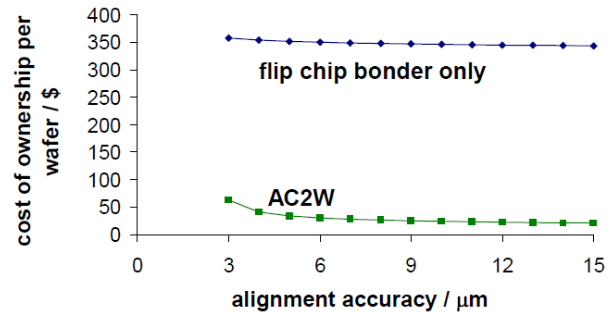


*Figure 4: Cost of Ownership comparison of Flip chip bonder only and AC2W bonding proces.*

## SUMMARY

Advanced bonding techniques for photonic integrated ciruits or heterogenous integration in general can add tremendous benefit for device fabrication and production costs. In particular plasma activation for wafer fusion bonding enables low temperature processes thus avoiding high bonding temperatures and reducing thermal stress or outgassing issues.

Wafer level chip to wafer bonding as shown with the AC2W process are a significant progress for cost of ownership models. Compared to other approaches like flip chip bonder only or wafer to wafer bonding it offers less material consumption at high yield and throughput and therefore is best suited for high volume chip to wafer production.

### ACKNOWLEDGMENT

LowTemp™ is a trademark of EV Group, St. Florian am Inn, Austria.

### KEYWORDS

Photonic integrated circuit, wafer bonding, plasma activation, chip to wafer

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