Surface Recombination and Performance Issues of Scaling Submicron Emitter on Type-II GaAsSb DHBTs

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Type-II GaAsSb DHBT has a staggered Type-II base collector band alignment, which eliminates the current blocking issue found in Type-I InP DHBT [1]. Due to its high breakdown voltage, high gain, and better linearity, Type-II DHBT has found wide applications in RF, mixed-signal IC, and communication instrumentations [2]. To push the Type-II GaAsSb DHBT operating frequency toward THz frequency range, lateral scaling is needed to reduce the device capacitance. However, as the emitter width of a DHBT is reduced, the current gain of the device will drop due to emitter peripheral surface recombination current. In this paper, we fabricated Type II GaAsSb DHBTs with different material structures and emitter widths. It is found that emitter peripheral recombination current can seriously reduce the DC current gain of Type-II GaAsSb DHBTs with different emitter and base designs. In addition, base contact resistance will also increase as the device is scaled down laterally, limiting the RF performance of scaled down device.

Figure 1 shows the DC current gain vs collector current density for devices with different emitter widths. The DHBT consists of an AlInP emitter, Doping graded GaAsSb base and InP collector. Due to emitter peripheral recombination current, current gain decreases as emitter width decreases. To extract emitter peripheral surface recombination current density coefficient K_{SURF}, we plot J_C/β as a function of P_E/A_E at a given collector current density. The total base current could be written as $J_C/\beta = J_{IN} + K_{SURF} \cdot P_E/A_E$, where J_{IN} is the intrinsic base current, P_E is emitter peripheral length, and A_E is the emitter area. Figure 2 shows the J_C/β vs P_E/A_E plot at collector current density J_C of 100 μA/μm^2. Figure 3 shows the extracted K_{SURF} value at different collector current densities for several different Type-II GaAsSb HBT structures. From Figure 3, we can see that K_{SURF} increases almost linearly as J_C increases for all four different Type-II GaAsSb DHBTs. Excessive emitter peripheral recombination current not only reduces current gain at low current density but also at high current density. For example, when $J_C = 4\ \mathrm{mA}/\mu m^2$, $J_{IN} = 100.8\ \mu\mathrm{A}/\mu m^2$ and $K_{SURF} = 21.7\ \mu\mathrm{A}/\mu\mathrm{m}$ for the doping graded base Type-II GaAsSb DHBT. For a 0.22x3 μm^2 device, $P_E/A_E = 9.76\ \mu m^{-1}$, and emitter peripheral surface recombination current is $K_{SURF} \cdot \frac{P_E}{A_E} = 211.7\ \mu A/\mu m^2$, which is more than twice that of J_{IN}. In order to reduce the emitter peripheral surface recombination current and increase DC current gain, an emitter ledge could be used similar to GaAs HBTs and InGaAs/InP DHBTs [3, 4].

In order to study the RF performance, we performed small signal measurement and modeling for devices with different emitter widths. The devices' S-parameters were measured using an Agilent E8364A PNA. The network analyzer was calibrated using an off-wafer calibration standard, with measurements of an on-wafer open and short to de-embed pad capacitance and inductance. The RF performance of a 0.38x5 μm^2 device is f_T/f_{MAX} = 470/535 GHz biased at J_C = 5 mA/μm^2 and V_{CB} = 0.65 V as shown in Figure 4. Table 1 lists the RF performance of three devices with different emitter and base-collector mesa widths. All devices are biased at J_C = 5 mA/μm^2 and V_{CB} = 0.65 V. To study the relationship between lateral scaling and RF performance, small signal modeling was performed. Figure 5 shows the small-signal model for the 0.38x5 μm^2 device with W_{BC} = 0.95 μm, biased at J_C = 5 mA/μm^2 and V_{CB} = 0.65 V. Important small-signal model parameters such as C_{BCi}, C_{BCx}, R_{Bi} and R_{Bx} are listed in Table 1. Comparing the two devices with A_E = 0.38x5 μm^2 W_{BC} = 0.95 μm and the device with A_E = 0.22x5 μm^2 W_{BC} = 0.8 μm, the intrinsic capacitance decreased from 1.4 fF to 0.9 fF. So, the f_{MAX} of A_E = 0.22x5 μm^2 W_{BC} = 0.8 μm increased from 535 GHz to 565 GHz, but the f_T decreased from 470 GHz to 450 GHz. This is because scaling of the extrinsic base-collector capacitance is not proportional to the scaling of emitter. So, we further scale down the base width. After reducing the base from 0.8 μm to 0.65 μm, f_T increased from 450 GHz to 480 GHz. However, the f_{MAX} decreased to 520 GHz, which is due to the increase in the base resistances as shown in Table 1. So, the high base resistance is the major limiting issue for the RF performance of the deeply scaled down DHBT device. The sheet resistance of the base is around 850 Ohm/sq. and contact resistivity is around 45 Ohm-μm^2. So, the base contact transfer length is around $L_T = \sqrt{45/850} = 0.23$ μm. Hence, as W_{BC} decreases to 0.65 μm, base contact width becomes smaller than the base contact transfer length, base resistance will increase dramatically. In addition to large base contact resistivity, there is also the misalignment problem as shown in Figure 6. When the base metal width becomes narrower and narrower, the misalignment will further increase the base resistance. So, as the device is scaled down, the base resistance, especially base contact resistance will limit the performance of f_{MAX}.

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[3] H. H. Lin, et al., Appl. Phys. Lett. 47, 5 (1985)
[4] Y. K. Fukai, et al., IEEE International Conference on Indium Phosphide and Related Materials (IPRM), Glasgow, Scotland, May 8-12, 2005, pp. 339-342.

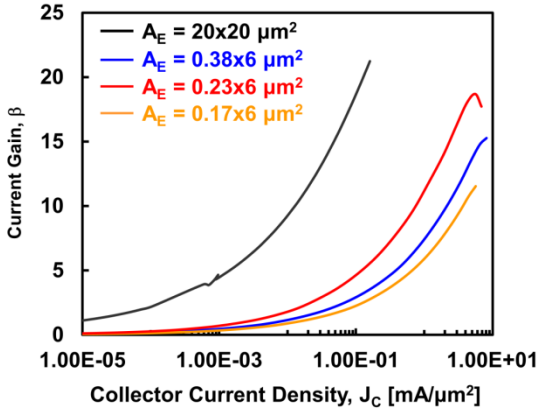

Fig. 1. (Color online) Current gain vs collector current density for devices with different emitter widths. The current gain decreases as the emitter width becomes smaller.

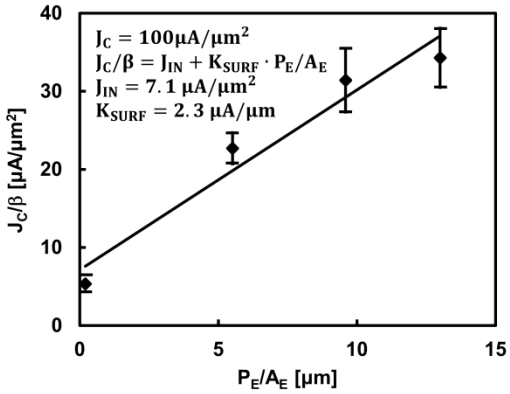

Fig. 2. (Color online) $J_C/\beta = J_{IN} + K_{SURF} \cdot P_E/A_E$ for different emitter widths at collector current density of J_C = 100 µA/µm^2.

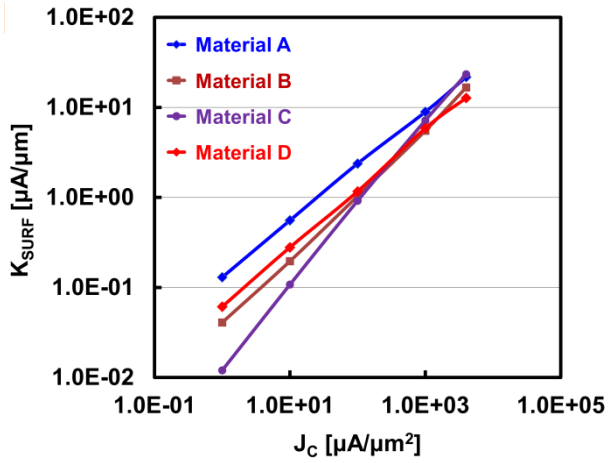

Fig. 3. K_{SURF} vs collector current density.

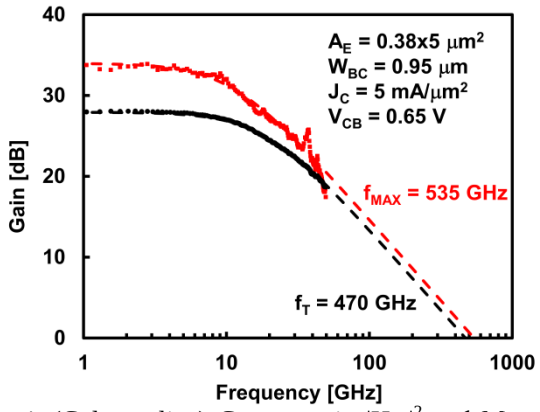

Fig. 4. (Color online) Current gain $|H_{21}|^2$ and Mason's Unilateral gain U as functions of frequency showing f_T/f_{MAX} = 470/535 GHz extracted using single-pole fitting method.

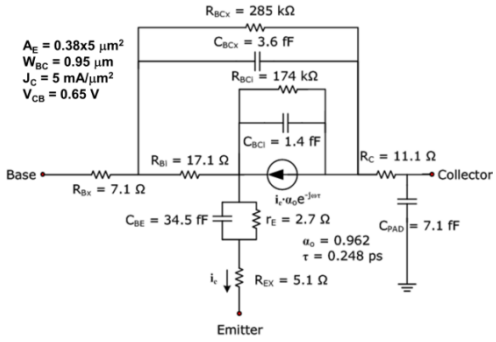

Fig. 5. (Color online) Small-Signal Model of a 0.38x5 µm^2 device.

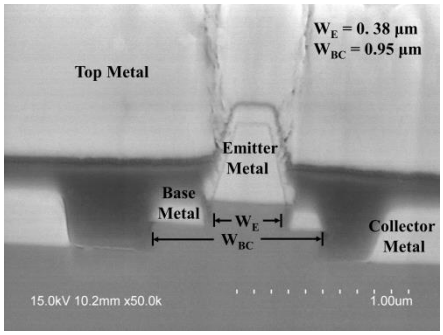

Fig. 6. Device SEM image of a SEM 0.38 µm device. The misalignment is about 50 nm.

	f_T (GHz)	f_{MAX} (GHz)	C_{BCi} (fF)	C_{BCx} (fF)	R_{bi} (Ohm)	R_{Bx} (Ohm)
A_E = 0.38x5 µm² W_{BC} = 0.95 µm	470	535	1.4	3.6	17.1	7.1
A_E = 0.22x5 µm² W_{BC} = 0.8 µm	450	565	0.9	3.5	16.9	6.8
A_E = 0.22x5 µm² W_{BC} = 0.65 µm	480	520	0.9	2.5	24.3	12.1

Table 1: Device Performances and Parameters