High Performance GaAs RF Switch with a P-Type Capping Layer

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Abstract

Due to the low insertion loss and the high linearity, a Junction Pseudomorphic High Electron Mobility Transistor (JPHEMT) is widely used for RF switches in wireless communications. In this paper, we offer a JPHEMT with a p-type capping layer from a gate region to source/drain regions for decreasing off-capacitance (C_{off}). The device parameters of the p-layer are optimized using device simulation technology to minimize the C_{off}. It has been demonstrated that gate-source breakdown voltage (BV_{gs}) is 11 V higher and C_{off} is 25 % lower than those of the JPHEMT. The obtained R_{on}*C_{off} product of 157 fsec is very competitive with those of RF switches utilizing conventional JPHEMT, silicon-on-insulator (SOI), and silicon-on-sapphire (SOS) technologies.

INTRODUCTION

We have been developing JPHEMT, which is widely used in RF switches for GSM, CDMA, UMTS, and LTE handsets due to its superior characteristics of insertion loss and linearity comparing to other switches [1]. Increasing the number of frequency bands for high speed wireless communications requires further improvement of the advantages of JPHEMT switches. Low insertion loss can be achieved by low on-resistance (R_{on}), and high isolation can be achieved by low C_{off}. Therefore, a low R_{on}*C_{off} product is critical to ensure low-loss RF switches. The R_{on} consists of a channel resistance from source electrode to drain electrode and source/drain contact resistance, which can be decreased by increasing the sheet electron concentration (N_s) at the InGaAs channel. On the other hand, C_{off} increases due to the reduction of the depletion layer width between the junction gate and the source/drain regions. Hence, there is a trade-off between R_{on} and C_{off}.

In this paper, we propose a new device structure of the JPHEMT with a p-type capping layer, which expands the depletion layer width for reducing C_{off} in the off-state without sacrificing R_{on} in the on-state. As a result, a low R_{on}*C_{off} product is realized.

DEVICE STRUCTURE AND FABRICATION

Figure 1 shows the schematics of the JPHEMT (structure A) and the new device structure (structure B). A double-doped AlGaAs/InGaAs channel was adopted for both structures. The structure B has the p-type capping layer located on the n-AlGaAs layer between the gate and the source/drain regions. In off-state, this p-layer works to deplete electrons at the InGaAs channel in the same way as junction gate works, resulting in large depletion layer width between the gate and the source/drain regions comparing to the conventional JPHEMT. A device fabrication for the structure B was started with a recess etching of the epitaxially grown p-layer of the source/drain ohmic electrode regions. Then, both structure A and B adopted a same fabrication process as follows. A SiN film was deposited and opened as a mask for Zn diffusion to form the junction gate region, followed by a device isolation using ion implantation. The gate and the source/drain electrodes were formed using Ti/Pt/Au and AuGe/Ni/Au metals, respectively. Finally, gate resistors and gold plating interconnects were formed.

RESULTS AND DISCUSSION

Using device simulation technology, we studied the contribution of the p-layer to the C_{off} behavior. The electron concentration profiles of the structure A and B at the gate-source bias voltage (V_{gs}) of -10 V are shown in Fig. 2. The InGaAs channel between the gate and the source region of the structure A accumulates electrons. However for the structure B, electrons at the channel beneath the p-layer are depleted. Therefore, the depletion layer width between the gate and the source region of the structure B is larger than that of the structure A. Figure 3 shows the simulated relation between N_s at the channel and the R_{on}, C_{off}, and R_{on}*C_{off} product, that are normalized based on the values of the structure A at N_s of $3.6\text{x}10^{12}$ cm^{-2}. The impact of the p-layer to the R_{on} seems small, especially for the high N_s, since the thickness of the n-AlGaAs is sufficiently large to prevent the electron depletion at InGaAs channel in the on-state. Although C_{off} increases with N_s, the structure B shows the significant decrease of C_{off} comparing to the structure A. We confirmed that the structure B has an advantage of R_{on}*C_{off} product due to low C_{off} and comparable R_{on} to the structure A. The DC characteristics and the small signal characteristics of both structures were measured at room temperature using a parameter analyzer and a network analyzer, respectively. The measured gate length and gate width of the transistors are 0.4 μm and 1 mm, respectively. In Table I, the threshold voltage (V_{th}) at the drain current of 0.5 mA/mm and the drain-source voltage of 0.1 V, on/off ratio, BV_{gs} at the I_g of 5

μA/mm, and C_{off} at 2 GHz are compared between the structure A and B. The BV_{gs} of the structure B is 11 V higher than that of the structure A due to the wide depletion size. The measured C_{off} of 153 fF/mm at V_{gs} of -10 V is 25 % lower than that of the structure A. Furthermore, C_{off} of 143 fF/mm at V_{gs} of -20 V was obtained, taking advantage of the high BV_{gs}. These results are in close agreement with the device simulation experiments as shown in Fig.3. In Table II, R_{on}*C_{off} products are compared among GaAs JPHEMT (this work), state of the art SOI, and SOS technologies [2]. Obtained R_{on}*C_{off} product is superior to other technologies.

CONCLUSIONS

We propose new device structure of JPHEMT with the p-type capping layer from the gate region to source/drain regions. Optimized structure using device simulation technology shows improved C_{off} without significant R_{on} increase, resulting in low R_{on}*C_{off} product. The fabricated new structure shows 25% lower C_{off} than that of the conventional JPHEMT without sacrificing R_{on}. The obtained R_{on}*C_{off} product is superior to those of RF switches based on other technologies.

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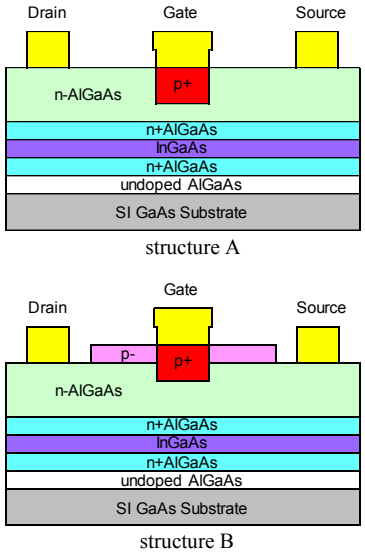

Figure 1. Schematics of conventional JPHEMT (structure A) and new device structure (structure B).

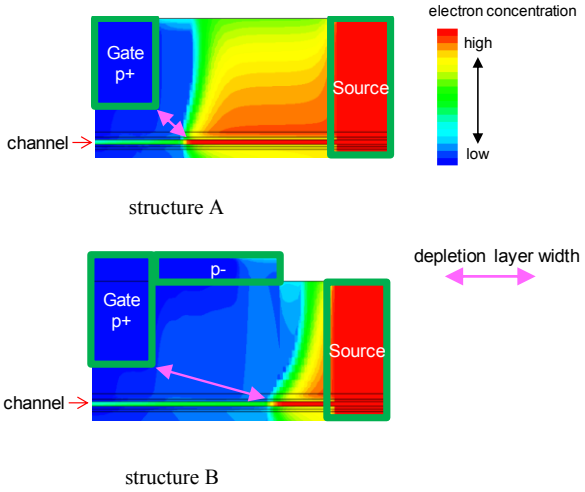

Figure 2. Electron concentration profiles at gate-source bias voltage of -10 V. Drain and source electrodes are grounded.

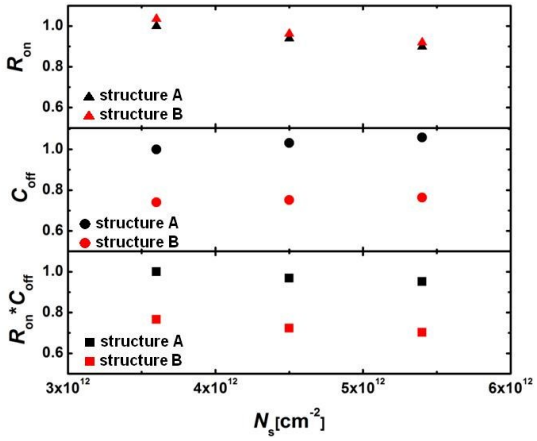

Figure 3. Simulated on-resistance (R_{on}), off-capacitance (C_{off}), and R_{on}*C_{off} product as a function of the sheet electron concentration (N_s) at the InGaAs channel.

Table I. Obtained parameters of structure A and structure B.

	structure A	Structure B
V_{th} [V]	-1.2	-1.2
On/off ratio	>10^7	>10^7
BV_{gs} [V]	-15	-26
C_{off} [fF/mm]	208 (V_{gs} -10 V)	153 (V_{gs} -10 V) 143 (V_{gs} -20 V)

Table II. Comparison of R_{on}*C_{off} product of GaAs JPHEMT, SOI, and SOS technologies.

	GaAs JPHEMT (This work)	SOI	SOS
R_{on}*C_{off} [fsec]	157	200	270