

## High-performance normally-off GaN MIS-HEMTs with dual gate insulator employing PEALD SiN<sub>x</sub> interfacial layer and RF-sputtered HfO<sub>2</sub>

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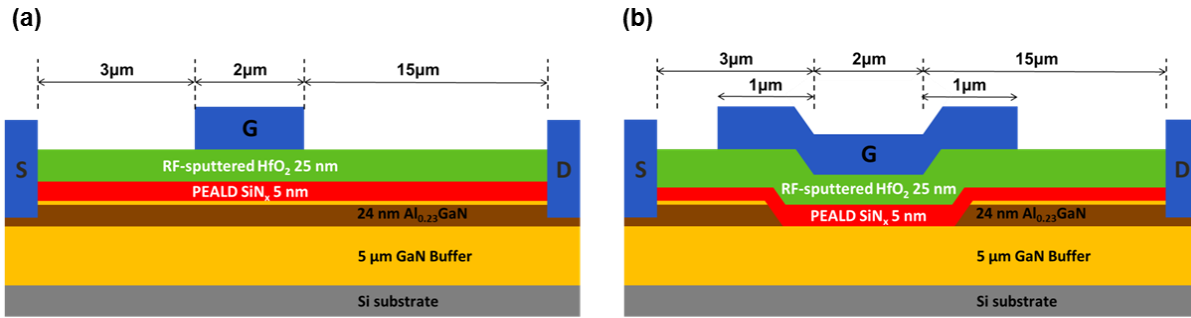
Gate insulator is the key technology in GaN-based metal-insulator-semiconductor high electron mobility transistors (MIS-HEMTs). Various dielectric materials were tried for gate insulator, such as SiO<sub>2</sub>, SiN<sub>x</sub>, Al<sub>2</sub>O<sub>3</sub>, AlN, HfO<sub>2</sub>, ZrO<sub>2</sub>, La<sub>2</sub>O<sub>3</sub>, and Ta<sub>2</sub>O<sub>5</sub> [1]. Among these materials, high-*k* dielectrics with  $k > 20$  have advantages for good channel controllability which leads to low OFF-state leakage current, high ON-state current, high ON/OFF current ratio, and low sub-threshold slope. However, there are many interface related problems in GaN MIS-HEMTs employing high-*k* dielectric, such as large amount of hysteresis, forward biased gate leakage current, and current collapse. In order to improve the interface quality, therefore, recent studies on the interfacial layer underneath the high-*k* dielectric were performed [2], [3], and these studies mean that need for good interfacial layer in GaN MIS-HEMTs is becoming increasingly necessary. In this work, we have developed a novel SiN<sub>x</sub>/HfO<sub>2</sub> dual gate insulator configuration for gate recessed normally-off GaN MIS-HEMTs. High quality very thin (5 nm) SiN<sub>x</sub> film deposited by plasma enhanced atomic layer deposition (PEALD) was applied as an interfacial layer under the RF-sputtered HfO<sub>2</sub> high-*k* dielectric.

The employed epitaxial structure included a 4 nm undoped GaN cap, a 24 nm undoped Al<sub>0.23</sub>Ga<sub>0.77</sub>N barrier, a 1 nm AlN spacer, and a 5 μm undoped GaN buffer layer on Si (111) wafer. Threshold voltages were -5.65 and +1.65 V when defined at the drain current of 1 mA/mm for normally-on and normally-off devices, respectively. The maximum drain currents of the normally-on and normally-off devices were 650 and 500 mA/mm, respectively. The maximum transconductance ( $g_{m,max}$ ) was also as high as 120 and 170 mS/mm for normally-on and normally-off devices, respectively. Due to good channel controllability enabled by dual gate insulator including a high-*k* dielectric material, the off-state drain leakage current was extremely small (lower than 10<sup>-9</sup> A/mm), and thus very high ON/OFF drain current ratio (~ 10<sup>9</sup>) and low subthreshold slope (~ 85 mV/dec) were obtained for both devices. The specific ON-state resistances ( $R_{ON,sp}$ ) were calculated from the slope of the linear regime in I<sub>D</sub>-V<sub>D</sub> curves, and the values were 1.79 and 1.84 mΩ·cm<sup>2</sup> for normally-on and normally-off devices, respectively. The capacitance-voltage (C-V) characteristics for both devices were measured, and the recessed device exhibited ~ 300 mV hysteresis. On the other hand, negligible C-V hysteresis was observed in non-recessed device. Therefore, it is suggested that the increased in on resistance and C-V hysteresis of the normally-off device was affected by gate recess etching damage. The breakdown voltage of the normally-off device was measured, and the value was as high as 900 V at the drain leakage current of 0.1 μA/mm with V<sub>GS</sub> = 0 V. The hard breakdown occurred at V<sub>D</sub> = 990 V. Benchmarked  $R_{on,sp}$  versus breakdown voltage plots including other reported normally-off GaN MIS-HEMT data are shown, which demonstrates the excellent performance of GaN MIS-HEMTs fabricated in this work.

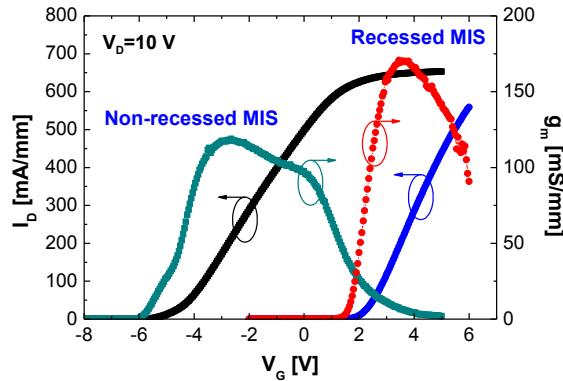
[1] R. D. Long et al., *Materials*, vol. 5, pp. 1297-1335, 2012.

[2] M. Van Hove et al., *IEEE Electron Device Lett.*, vol. 33, pp. 667-669, 2012.

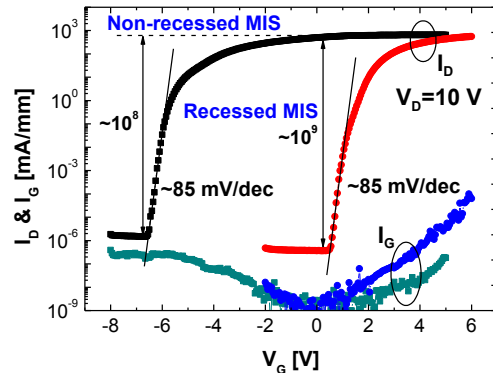
[3] J. Kashiwagi et al., *IEEE Electron Device Lett.*, vol. 34, pp. 1109-1111, 2013.



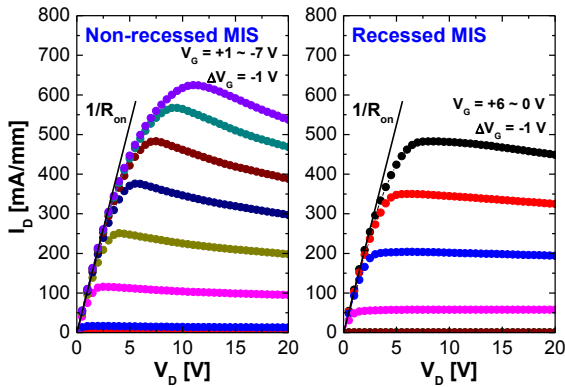
**Fig. 1:** Cross-sectional schematic of (a) non-recessed normally-on and (b) gate recessed normally-off GaN MIS-HEMT with 5 nm PEALD SiN<sub>x</sub> / 25 nm RF-sputtered HfO<sub>2</sub> as dual gate insulator structure.



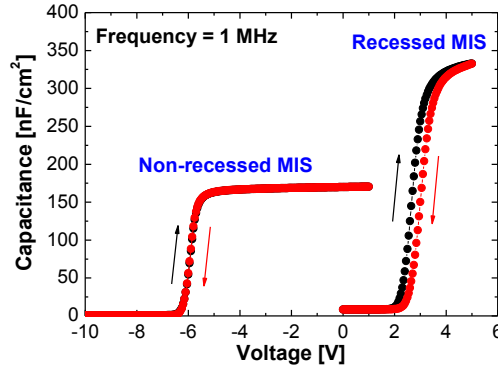
**Fig. 2** Linear scaled transfer characteristics of the non-recessed and gate recessed MIS-HEMTs with the drain current ( $I_D$ ) and the transconductance ( $g_m$ ).



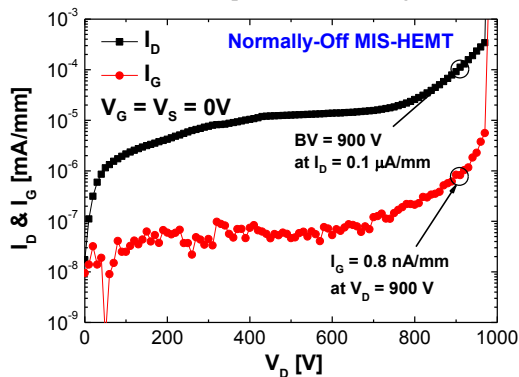
**Fig. 3** Log scaled transfer characteristics of the non-recessed and gate recessed MIS-HEMTs with the drain current ( $I_D$ ) and the gate current ( $I_G$ ).  $I_{ON}/I_{OFF}$  ratio and subthreshold slope are also shown.



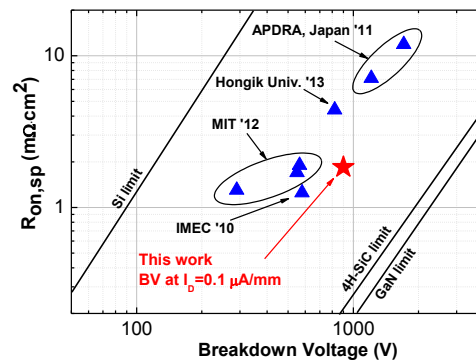
**Fig. 4**  $I_D$ - $V_D$  characteristics of normally-on and normally-off GaN MIS-HEMTs were plotted. Specific ON-state resistance was calculated from the slope of the linear regime.



**Fig. 5** Capacitance-voltage characteristics of non-recessed and recessed MIS capacitor measured with frequency of 1 MHz.



**Fig. 6** Off-state breakdown characteristic of the fabricated normally-off GaN MIS-HEMT is shown.



**Fig. 7**  $R_{ON,sp}$  versus BV is plotted with other reported normally-off GaN MIS-HEMTs.